Study of the Performance of the CMS Endcap Muon Trigger

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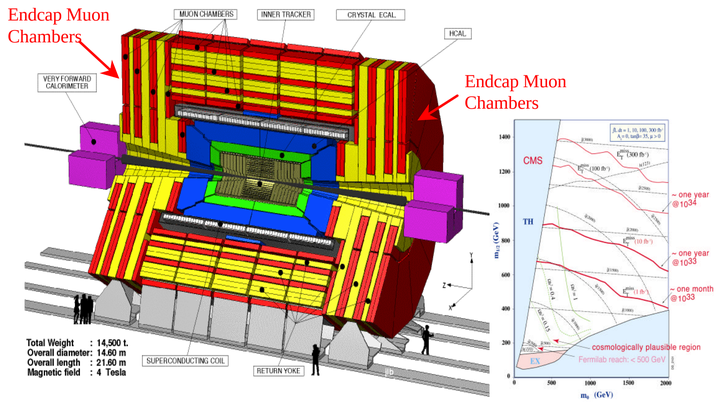
Compact Muon Solenoid (CMS)



SUSY parameter space at LHC

Cathode Strip Chambers on Muon Endcap

The Cathode Strip Chambers (CSCs) of the muon endcap system are ionizing drift chambers, consisting of six layers of radial cathode strips and anode wires approximately orthogonal to the strips. An ionizing gas mixture fills the chambers across which a high voltage is applied so that when ionizing particles pass through the camber, the free electrons collect on the anode wires and an image current forms on the cathode strips. On-chamber electronics measure this current and create a Local Charged Track (LCT), which is then sent to peripheral crate electronics. Peripheral crate electronics make a local trigger decision by combining the anode and cathode LCTs and pass this information to a global trigger. A response from the global trigger (Level 1 Accept -- L1A) prompts the peripheral crate electronics to read out the information pertaining to the LCT.

As shown to right, the coordinates of CMS are cylindrical with the beam axis taken as the z-axis. The cathode strips precisely measure the position of a charged track in phi and the anode wires measure rapidity (eta).

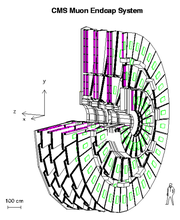
The basic requirements of the local CSC trigger system* are:

• LCT efficiency larger than 95% to achieve a high overall track finding efficiency (subdivided into CLCT pattern finding, ALCT pattern finding, ALCT bunch crossing assignment and ALCT-CLCT time coincidence).

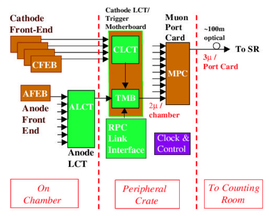
• The bend coordinate measured to an RMS accuracy of 0.15 strips (typically 1 mm), enabling a momentum measurement up to 100 GeV/c.

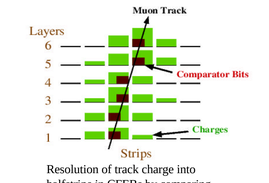
• System must be able to perform in the presence of high background hit rates.

*Source: CMS Trigger TDR, Ch 11.



Muon Endcap Local Trigger Electronics





Resolution of track charge into halfstrips in CFEBs by comparing charge to left and right of peak.

• CFEB (Cathode Front-End Board): Amplifies cathode strip signals and creates parallel, independent trigger and data paths. Analogue charge information is stored in a switch capacitor array and digitized for readout. Cathode charge information also passes through comparators, creating digital bits sent to the TMB for determination of cathode LCT (CLCT). These digital bits are resolved into half-strips using the charge distribution of the analogue information (see bottom left).

• AFEB (Anode Front-End Board): Contains a discriminator to digitize anode information, which is then sent to ALCT board.

• ALCT (Anode LCT): Finds up to two anode LCT hit patterns and determines muon bunch crossing using a multiple-layer coincidence timing technique. Sends ALCTs to TMB for local trigger decision.

• TMB (Trigger Mother Board): Finds up to two cathode LCT patterns, then checks for a time coincidence between ALCTs and CLCTs. If a coincidence is found TMB combines the LCTs and sends the best two LCTs to the MPC.

• MPC (Muon Port Card): Collects LCTs from every TMB in sector and chooses best three. Sends this information to global trigger system (Sector Processor, Sector Receiver).

*Source: CMS Trigger TDR, Ch 11.

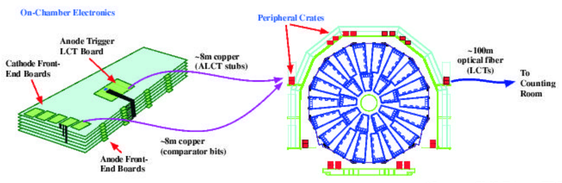
Muon Endcap Local Trigger Electronics and Data Acquisition (DAQ) Electronics

• CCB (Clock and Control Board): Provides the interface of the CSC system with the global CMS Trigger, Timing and Control (TTC) system. Distributes necessary signals for operation of CSC system (eg. Level 1 Accept -- L1A).

• DMB (DAQ Mother Board): Upon arrival of L1A, collects data from ALCT, TMB and CFEBs, containing ALCTs, CLCTs and analogue cathode information from a single CSC. Sends this event information to DDU.

• DDU (Detector-Dependant Unit): Upon arrival of L1A, collects data from all DMBs in muon endcap sector and sends information down global DAQ path.

Layout of electronics on muon endcap:

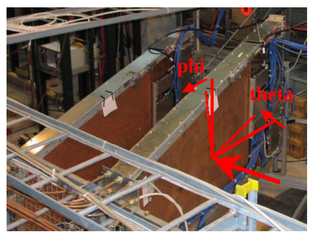


*Source: CMS Trigger TDR, Ch 11.

Description of conditions of test beam at CERN

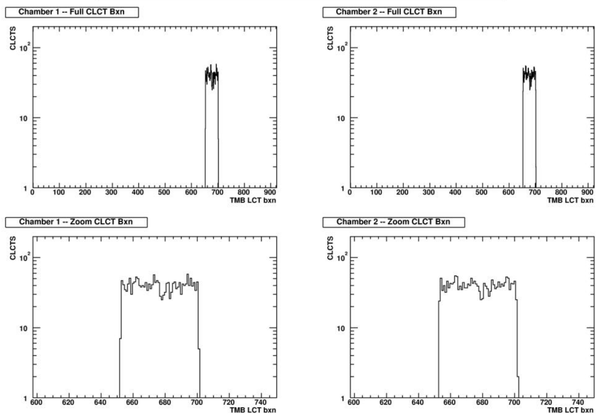
In May and June of 2003, the performance of the CMS endcap muon trigger was studied with the purpose of examining the system in LHC conditions before going into full production of the trigger hardware. The tests placed two CSCs in the X5A beam, which is a tertiary beam from CERN's SPS (400 GeV/c), providing a muon or pion beam of energy between 5 and 250 GeV within a spot size of a few millimeters (RMS) on the chambers. Collimators in the beam line allowed for control of the rate of particles. Three scintillation counters placed at least a few meters apart in front of and behind the chambers in the beam line provided an independent measurement of particle rate as well as a means of supplying the system with a L1A signal. The two CSCs were placed about a meter apart and nominally rotated 20^0 with respect to the perpendicular to the beam axis; they were nominally oriented vertically with respect to the floor (parallel to beam axis -- see right).

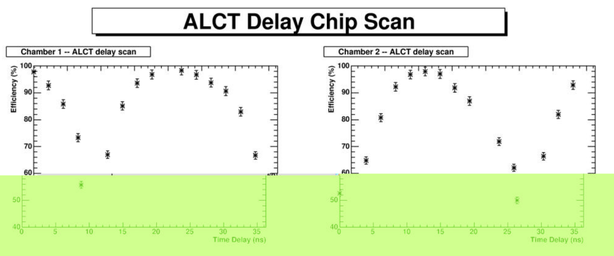
The test period was divided into two phases: one with beam of synchronous bunch structure and one without, where synchronous bunch structure ("structured beam") allows for a realistic determination of anode and cathode timing for bunch crossing identification. Structured beam refers to having 48 filled bunches in a 924 bx orbit -- the page below displays a measurement of the bunch structure at the test beam.



SPS Structured Beam Parameters:

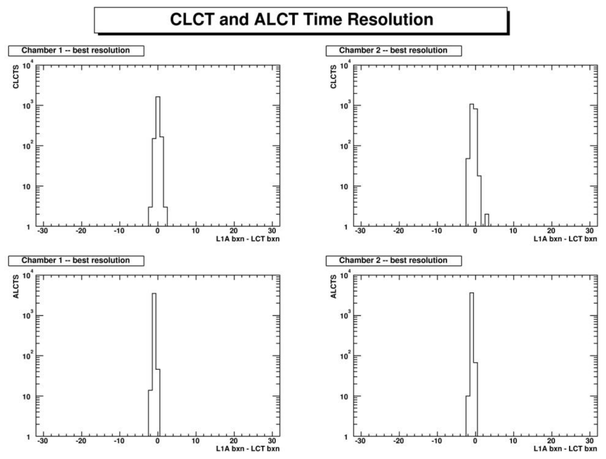
- beam clock = 24.95 ns (to 100 ppm)
- ~2.3 ns wide bunches
- ~16.8 s period for ramp/spill cycle
- ~2.6 s spill duration
- ~23 ms orbit period during spill
- 1 filled train per orbit
- 48 filled bunches in one train

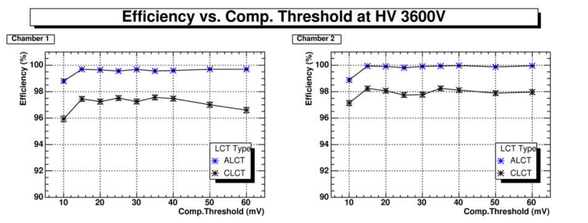




One of the most important functions of the ALCT board is to accurately determine the time (in bxn) at which a LCT is formed. Due to the very high rate LHC conditions, precise timing resolution is required for track identification. Time resolution here refers to matching the bxn of the local LCT with the global L1A (modulo a constant offset).

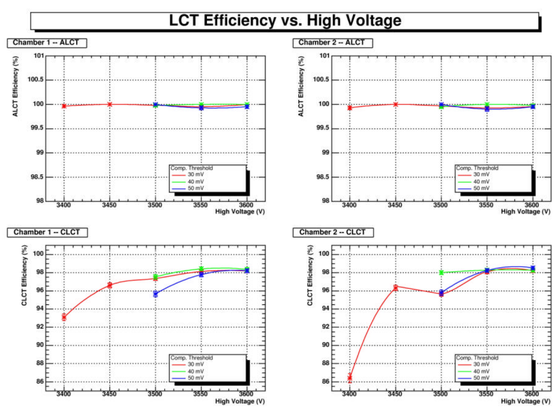
The ALCT board contains a delay chip for each wire group channel that it reads out. These delay chips delay the LCT signal in 2.2 ns steps. Using structured muon beam, a scan over the delay chip settings was preformed to find the best ALCT time resolution (see above). Efficiency in the above plots is defined as the number of LCTs in the peak bin divided by the total number of LCTs. The following page shows the time resolution for each chamber at their respective peak in efficiency and also typical timing resolution from the CFEBs. Note that the ALCT bxn is used for track identification -- it is not required for the time resolution of the CFEBs to be as good because the TMB matches the ALCT and CLCT.





The level of the cathode comparators for sending digital bit track information to the TMB was adjusted to determine the TMB's response to the presence of noise on the CLCT signal (assuming low threshold gives more noise).

A full study of the efficiency of chamber response as a function of high voltage was done during the initial setup of the chambers with cosmic muons. The results shown on the next page are the responses of the chamber around the high voltage giving maximum efficiency to find the efficiency of the CSCs in LHC conditions.



Explanation of Patterns and Quality in ALCT and TMB Logic

- ALCT Pattern: The ALCT finds tracks by applying a pattern mask over each key wire group along the full range of wire groups. The key wire group is defined as a single wire group on the 3rd layer (ly 2) of the chamber. There are two pattern masks allowing for two types of muons in the detector: collision muons, which originate from the interaction region, and accelerator muons, which travel parallel to the beam pipe. During the majority of the test beam, the ALCT was set to trigger only on collision muons with a wide range of angles (see Fig. 1 at right).

xxx__	ly 0
_xx__	ly 1
__x__	ly 2
__xx_	ly 3
__xxx	ly 4
__xxx	ly 5

Fig. 1 ALCT Pattern

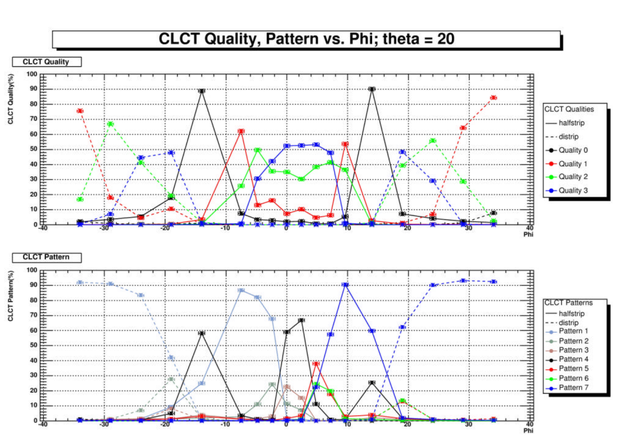
- TMB Patterns: The TMB finds tracks in a manner similar to the ALCT, except that the key halfstrip is on the 4th layer (ly 3). To allow for both high and low PT tracks, the TMB pattern finding separately applies the pattern masks to each key halfstrip and distrip, respectively. TMB pattern finding logic includes seven patterns: one straight-trough pattern and then varying degrees of bend in positive and negative phi direction (see Fig. 2 below).

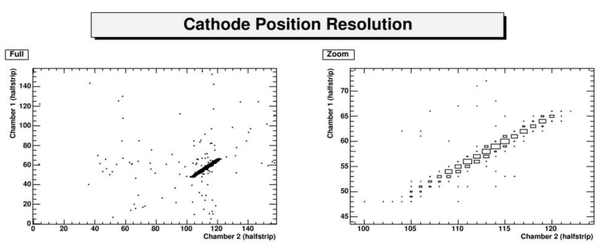
Fig. 2: TMB Patterns

pattern 1	pattern 2	pattern 3	pattern 4	pattern 5	pattern 6	pattern 7	
x___	_x__	x___	_x__	__x_	_x__	__x_	ly 0
x___	_x__	x___	_x__	__x_	_x__	__x_	ly 1
xx__	_x__	xx__	_x__	_xx_	_x__	_xx_	ly 2
_x__	_x__	_x__	_x__	_x__	_x__	_x__	ly 3
_xx_	__x_	_x__	_x__	_x__	x___	xx__	ly 4
__x_	__x_	_x__	_x__	_x__	x___	x___	ly 5

- Quality: In this presentation, the quality of LCTs from both ALCT and TMB refers to the number of layers with hits matching a pattern. The qualities are defined as follows:

quality 3 = 6 layers quality 2 = 5 layers quality 1 = 4 layers quality 0 = 0-3 layers



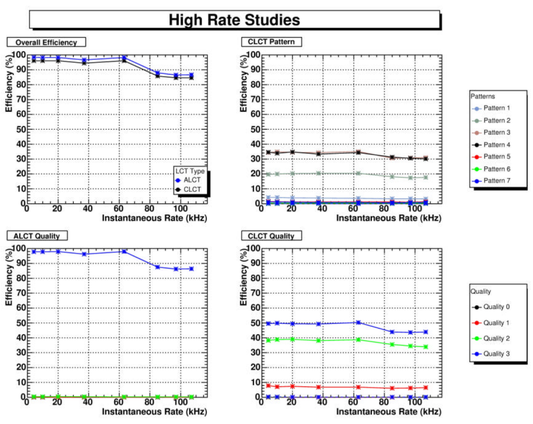


A scatter plot of the half strip position of the muon tracks in the two chambers as recorded in the TMB's CLCT data. Note the linearity of the plot, where the offset is due to the physical location of chamber 1 vertically higher (relative to the beam) than chamber 2. The width of the data gives an estimate of the cathode position resolution.

High Rate Trigger Study

This high rate trigger study was preformed by using collimators in the test beam line to control the rate of pions in unstructured beam. In the following study, the rate of particles passing through the cambers was measured by the coincidence of three scintillation counters, giving a scalar number of particles per spill from which the instantaneous rate was calculated.

Although the trigger rate (LCT rate) is very high, the readout through the data stream was limited to approximately 1.7 kHz per spill by controlling the L1A rate. Since the readout only occurs for every L1A pulse, the DAQ could still operate at the high LCT rate.



Conclusions

Performance of local CSC trigger meets or exceeds LHC requirements:

- Achieved 99% efficiency in ALCT time resolution of an ALCT to a single bxn.
- Achieved 99% efficiency in ALCT of finding tracks with LHC trigger parameters.
- Achieved 98% efficiency in TMB of finding CLCTs with LHC trigger parameters.
- TMB patterns properly identify phi angle of tracks.
- Trigger system performs well up to much higher rates than expected at LHC.

Suggestions for further study:

- Test ALCT with collision and accelerator muon patterns
- Test communication between TMB and MPC