Hybrid Pixel Detectors for a Linear Collider Experiment

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The Vertex Tracker for the future linear collider must be able to provide:

- a track impact parameter resolution of

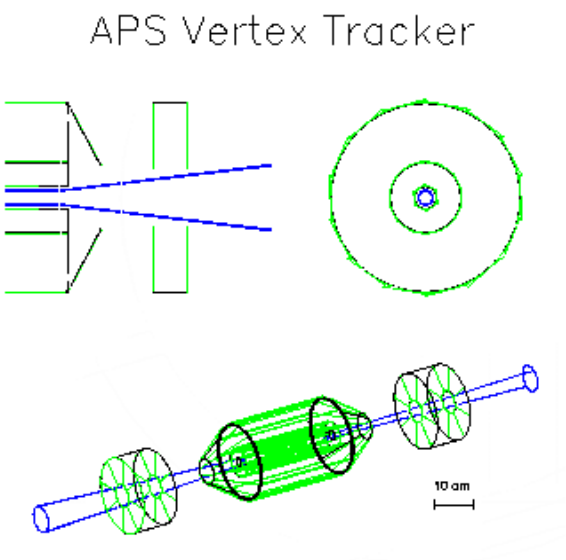
$$5\mu m \oplus \frac{10\mu m}{p \cdot sin^{3/2}(\theta)}$$

in the R-Φ projection and a similar resolution in R-Z

•Time stamping of each bunch crossing for background reduction ("easy" at TESLA, with a BCO every 330 ns)

- Single cell size less than 150 x 150 μm to keep the occupancy from jets below 1 %

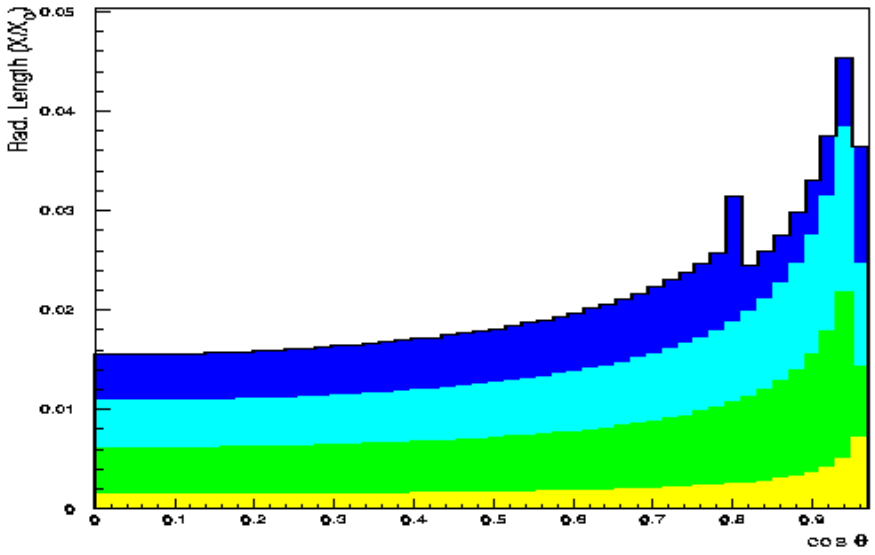
The Pixel Vertex Tracker Design



Layer	R (cm)	z (cm)
I	1.2	$\pm$ 5.5
II	3.5	$\pm$ 14.5
III	10.0	$\pm$ 14.5

- two independant half-shells for installation with beam-pipe *in situ*;
- pixel modules installed on thin diamond or diamond-coated carbon fiber;

Material Budget for the Pixel Vertex Tracker

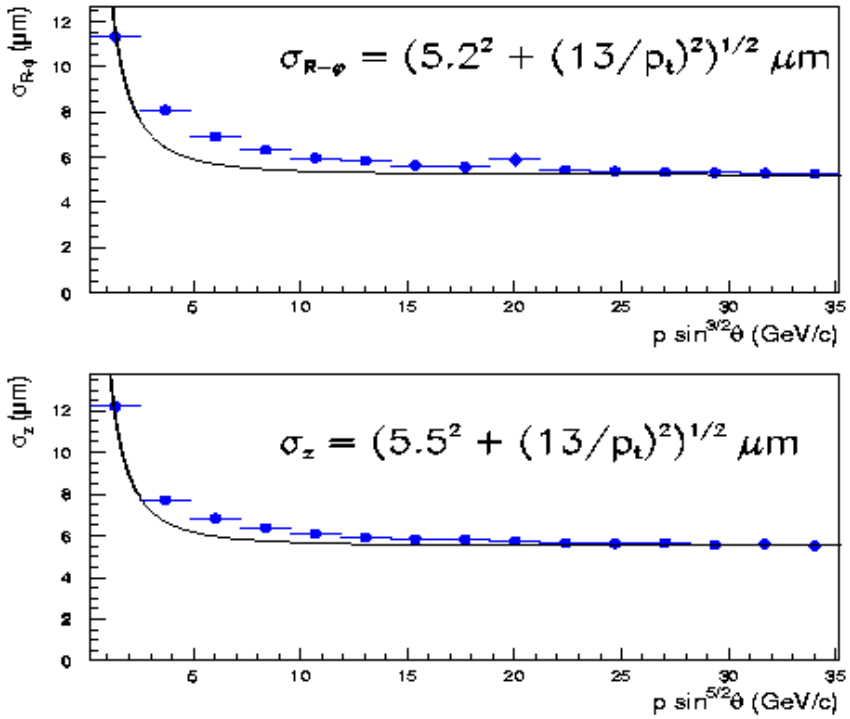


	R (cm)	Mat.	X (cm)	X_0 (cm^{-1})	X/X_0 (%)
Beam-pipe	1.0	Be	0.0500	35	0.15
APS+VLSI+Kapton	1.2	Si	0.0250	9.4	0.37
Support	1.2	CF	0.0240	25	0.10
APS+VLSI+Kapton	3.5	Si	0.0250	9.4	0.37
Support	3.5	CF	0.0240	25	0.10
APS+VLSI+Kapton	10.	Si	0.0250	9.4	0.37
Support	10.	CF	0.0240	25	0.10
Total					1.60

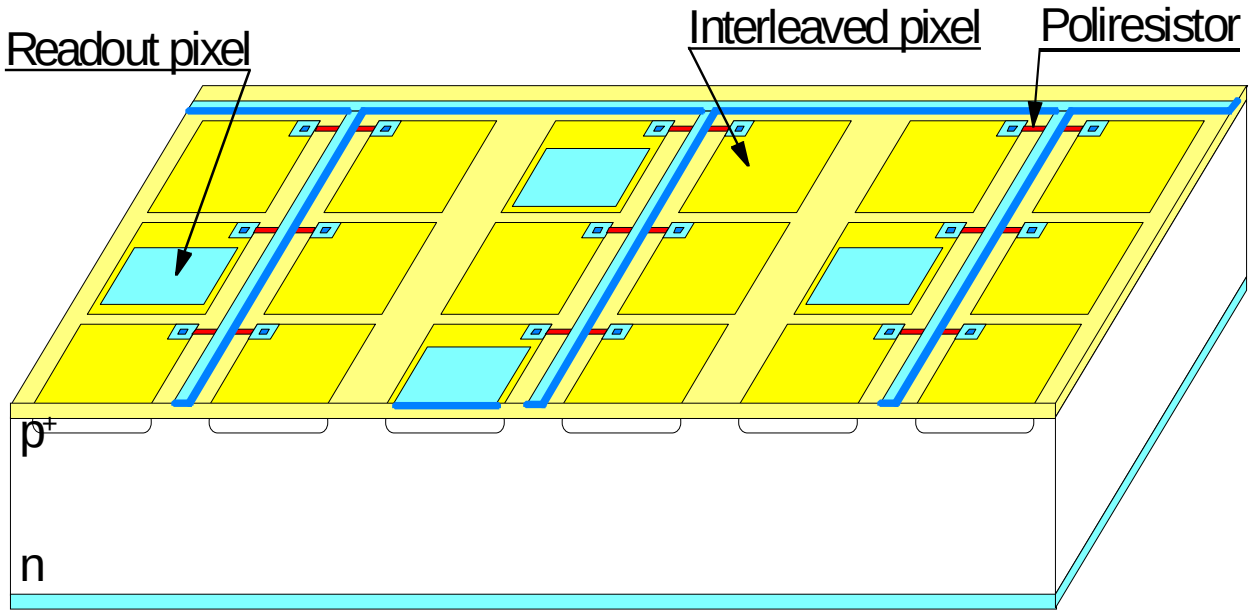
Asymptotic Impact Parameter Resolution for different Pixel Single Point Accuracies

σ_{point}	σ_{IP}^{asympt}
4.	3.7
7.	**5.5**
10.	7.5
13.	9.5

Impact Parameter Resolution vs. p



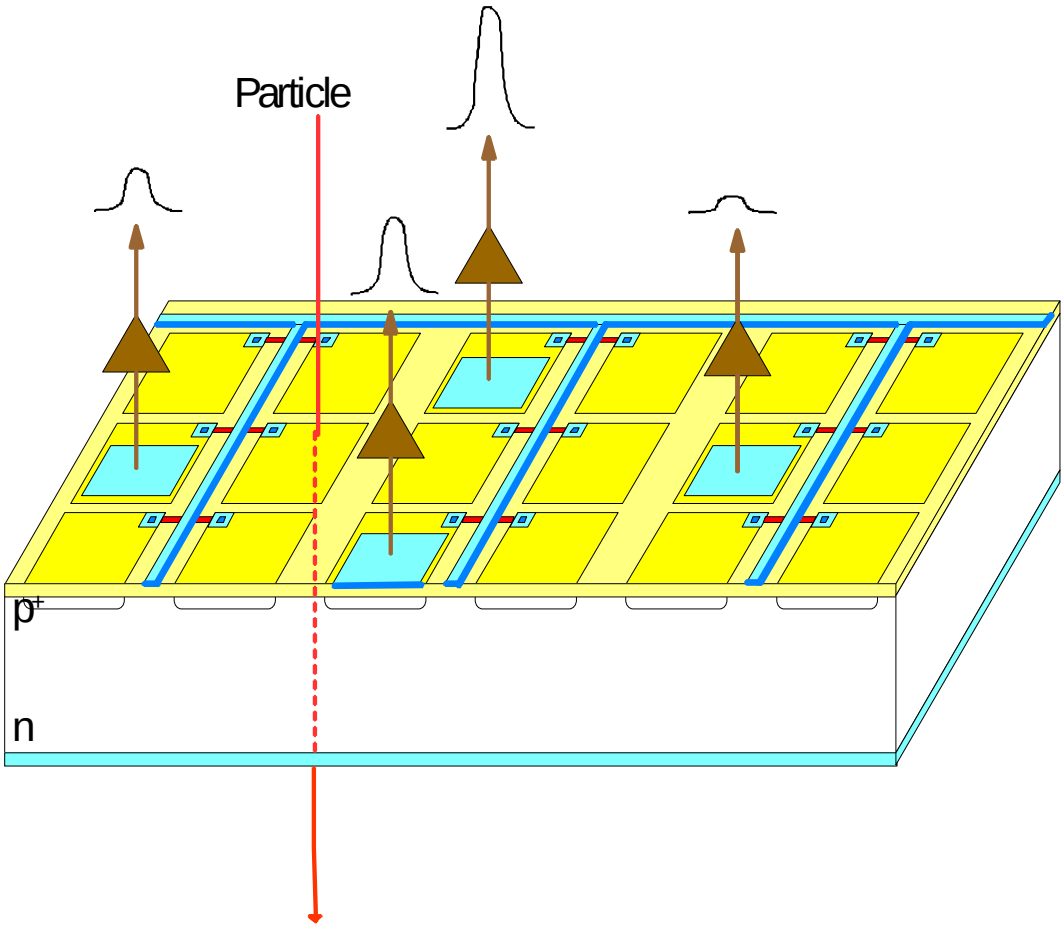
Hybrid detector with interleaved pixels between the output nodes



readout pitch = n x pixel pitch

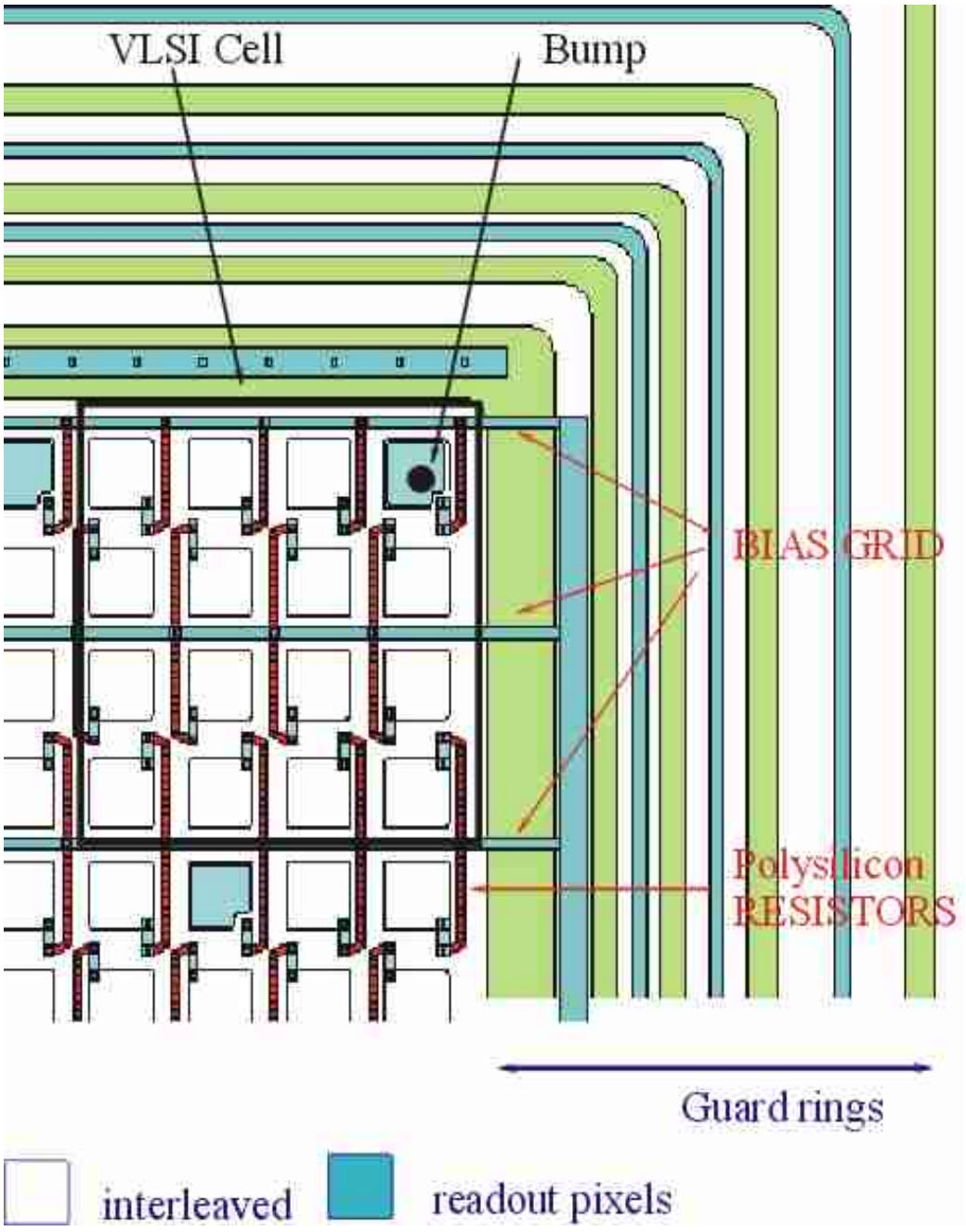
Large enough to house the VLSI front-end cell

Small enough for an effective sampling



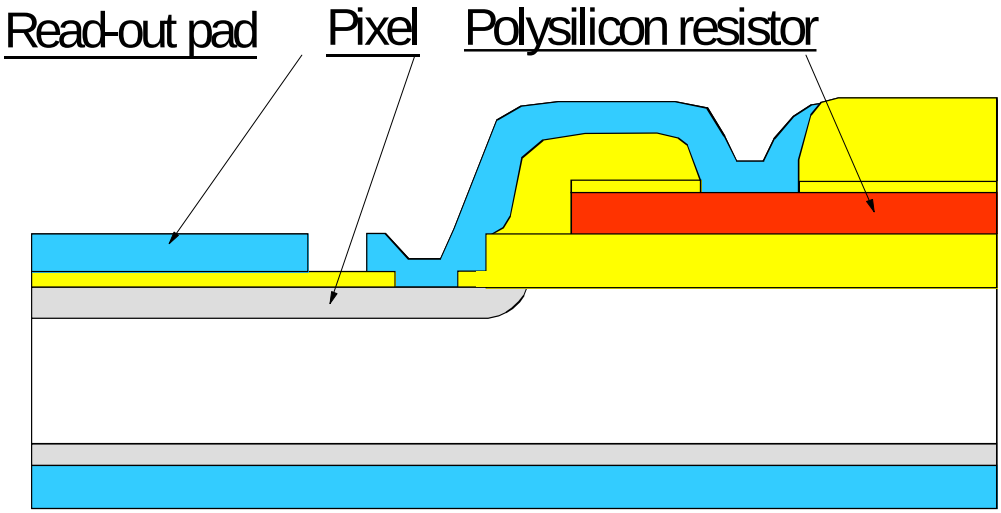
Due to the capacitive charge division a particle will induces a signal on the surrounding pixels beyond the diffusive charge carrier spread

Layout of the proposed Pixel sensor



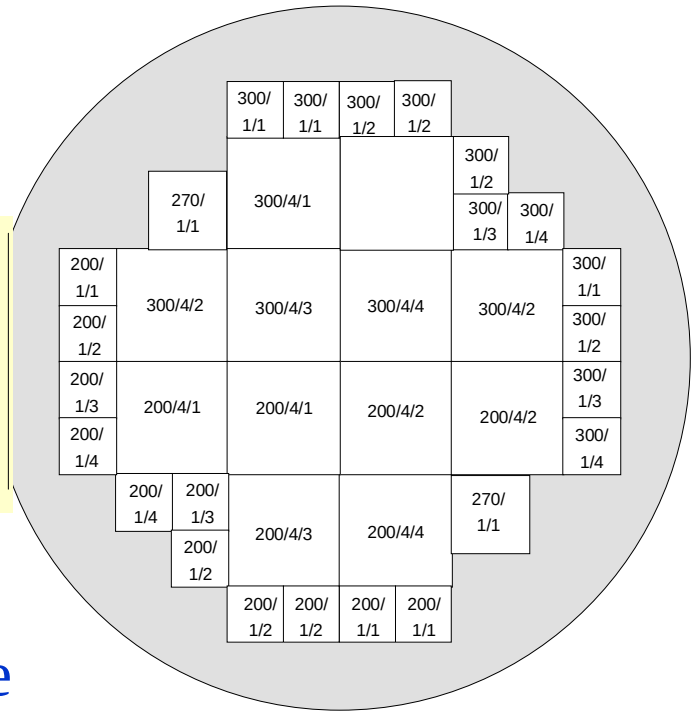
Technology process:

- 1 polysilicon layer
- 1 metal layer



Detectors were fabricated
by the Institute of Electron Technology
in Warsaw, Poland

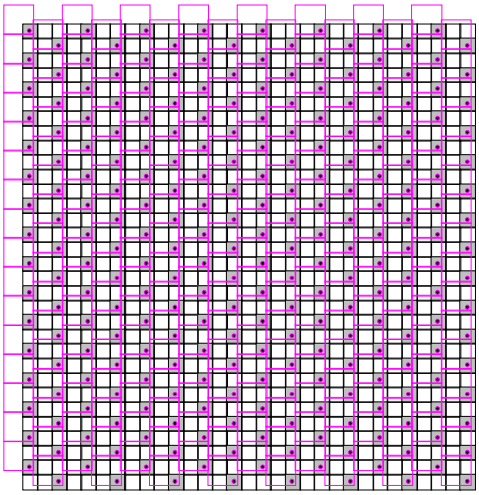
4” wafer with:



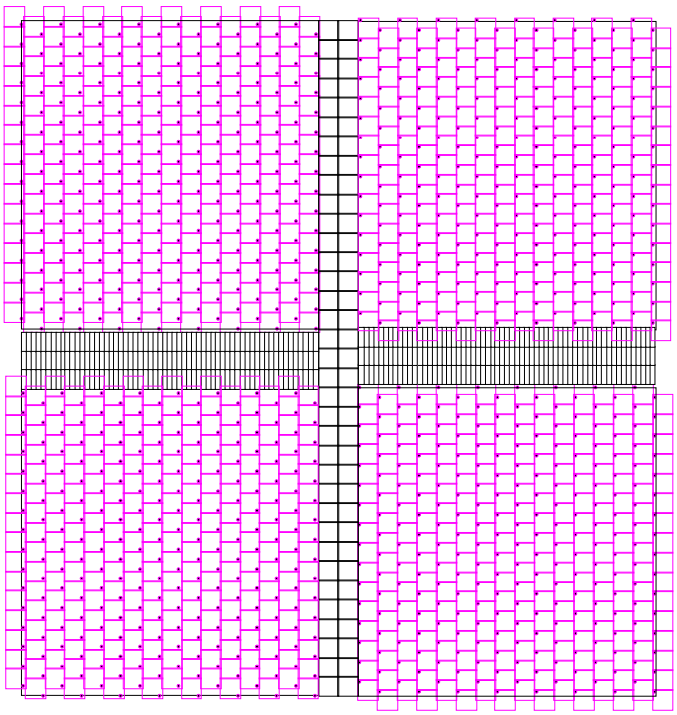
- Detectors for single and four chip structure

- Two readout pitches (200 and 300 μm) in both dimensions

- 36 detector structures with 17 different configurations (pitch, # of interleaved pixels)

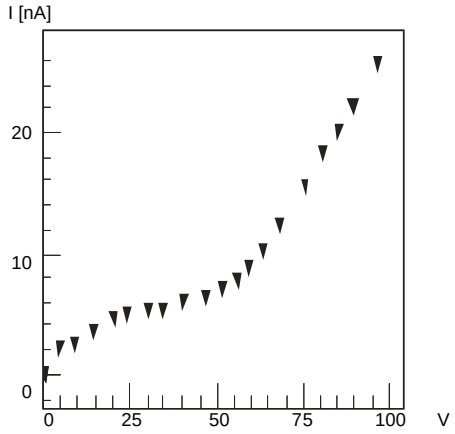


One chip detector structure

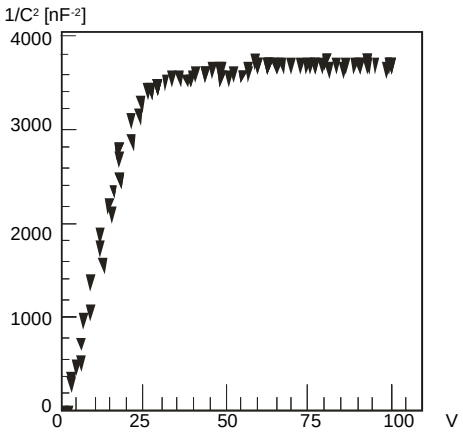


Four chips detector structure

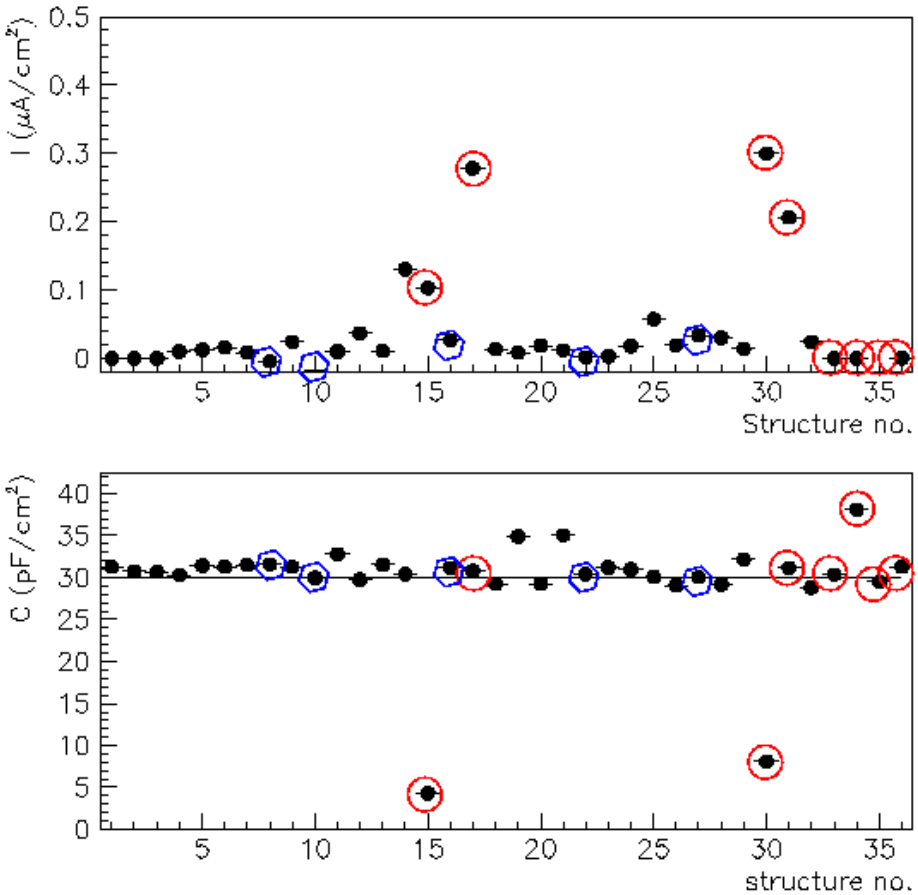
I-V and C-V characteristics



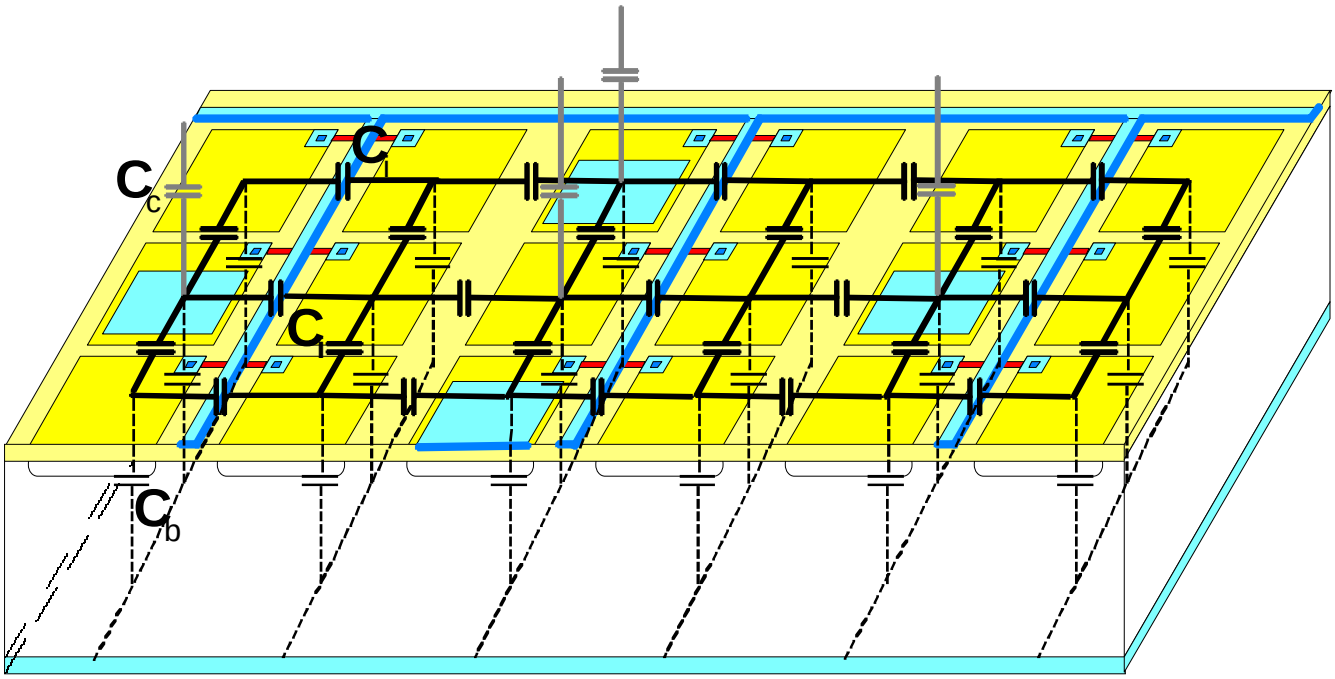
Typical current for full depletion:
~10-20 nA/cm^2



Leakage current and capacitance capacitance at full depletion voltage for all 36 structures in one of the wafers



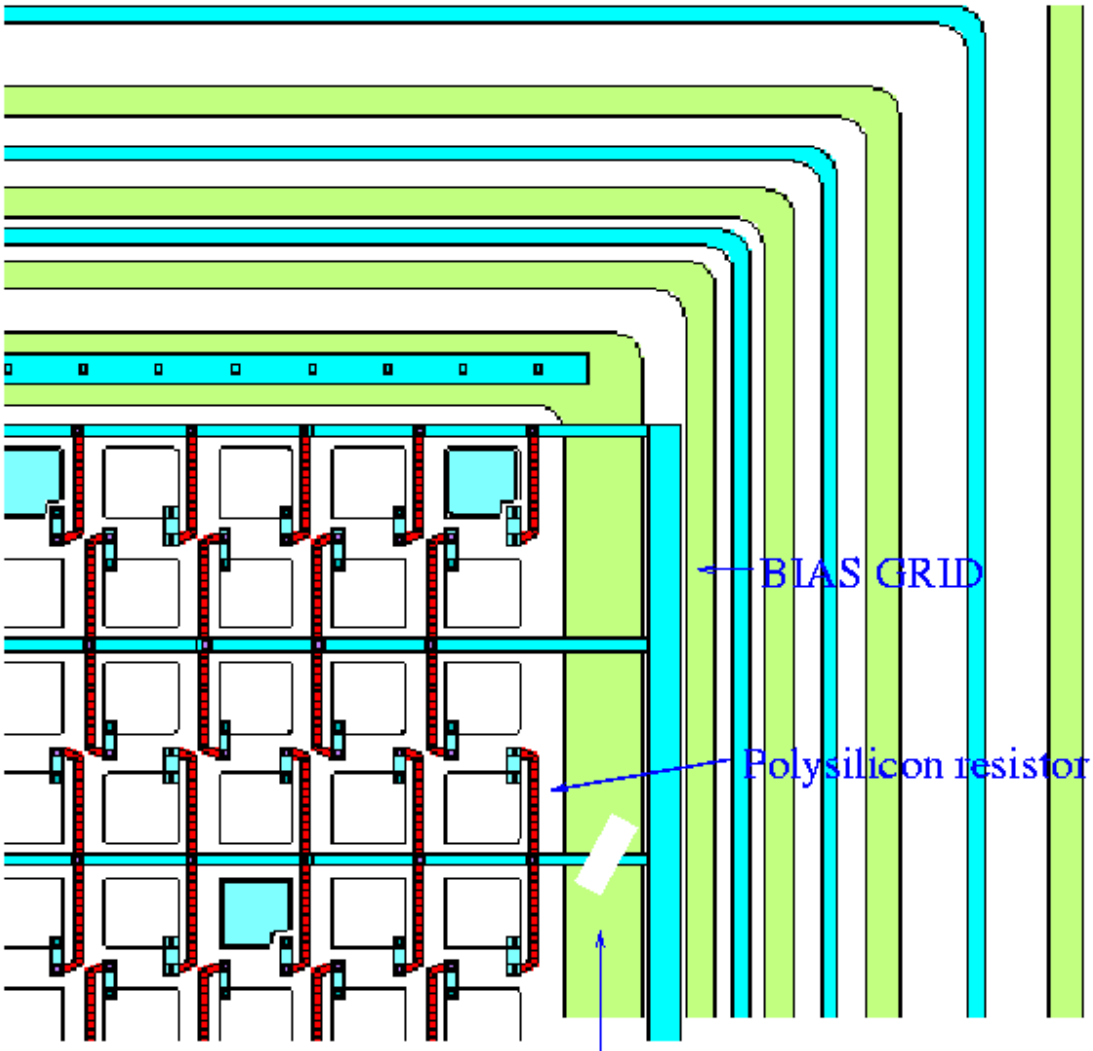
Interpixel and Backplane Capacitance



The detector may be modeled as a network defined by:
C_b – backplane capacitance
C_i – interpixel capacitance
C_c – coupling capacitance

The expected charge loss depends on the ratio between the interpixel and backplane capacitance

As the single pixel capacitances are expected to be ~ 10 fF
a trick based on the detector layout was conceived:



- the metal line connecting a pair of columns to the bias grid was SCRATCHED, isolating it from the rest of the detector

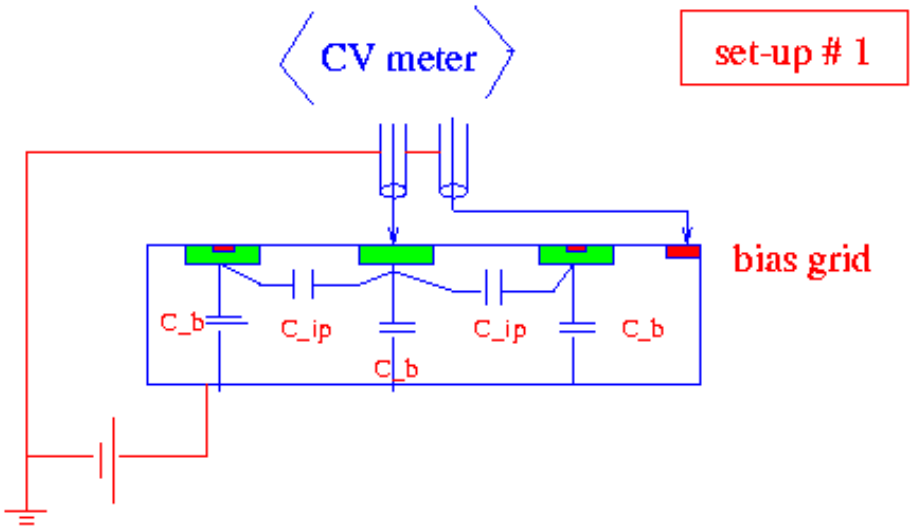
=> the parallel capacitance for 2 x no. pixels / column is measured

- the detector is biased through the guard ring

The measurements were performed on undiced wafers, previously tested (I-V and C-V curves) relying on a

- Keithley 2410 power supply
- HP4280 CV meter, operating at 1 MHz

Since these measurements are dominated by possible systematics, two different set-up's and three different measurements protocols were defined, to cross check the results:



- the power supply is in series with the CV meter
- they both share the same ground
- the ground is made to coincide with the detector backplane

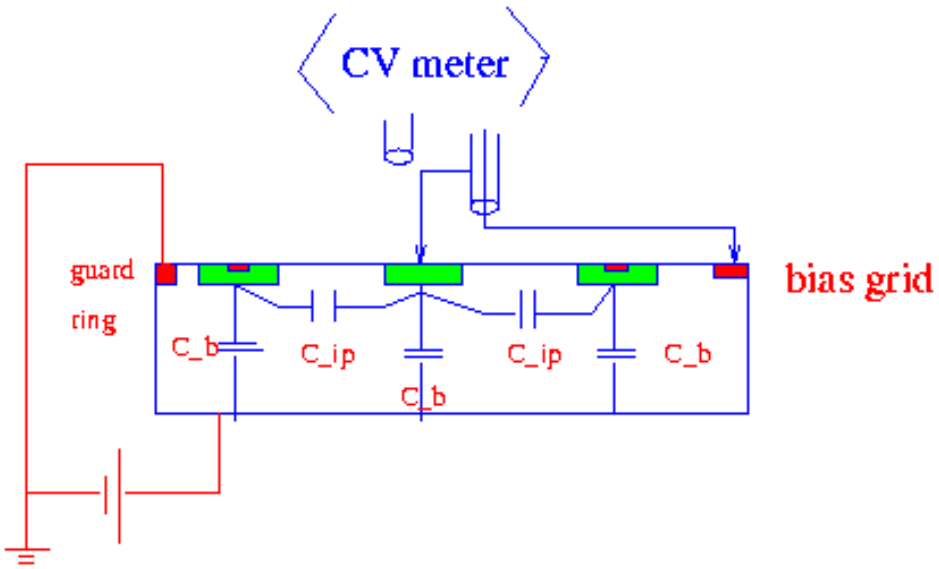
→ Backplane capacitances appear as a contribution to the stray capacitance to ground

set-up # 2 defining protocol # 3:

- the detector is biased via the guard ring

- the CV meter ground is made to coincide with the probe tip on the interrupted line(s)

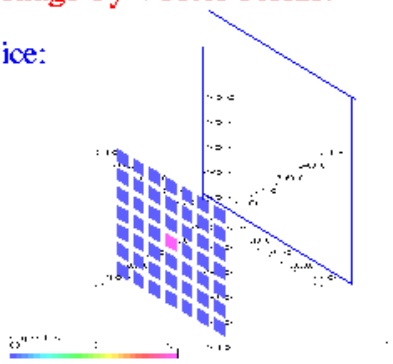
- the capacitance to ground is measured



→ the series of the interpixel and backplane capacitance is measured and the value can be compared to the output of the other protocols

Estimate of the capacitances by solving the Laplace equation using TOSCA, a routine of the OPERA package by Vector Fields:

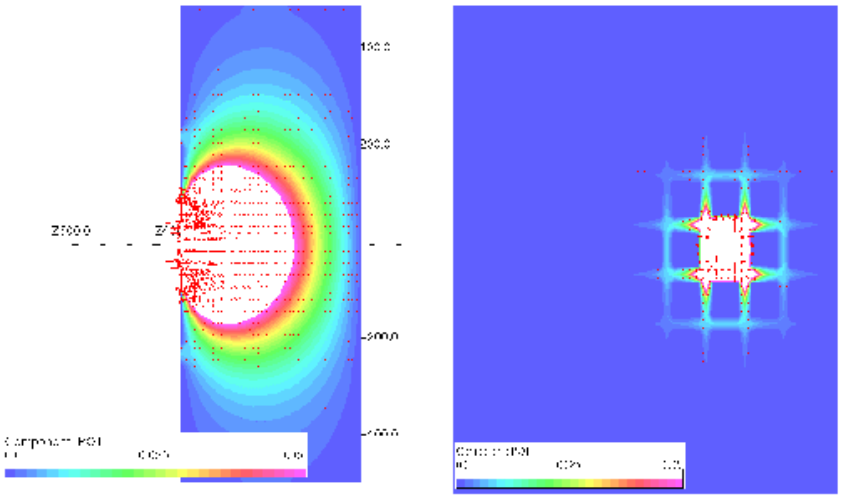
- describe the geometry of the device:
  - array of 7 x 7 pixels facing the backplane



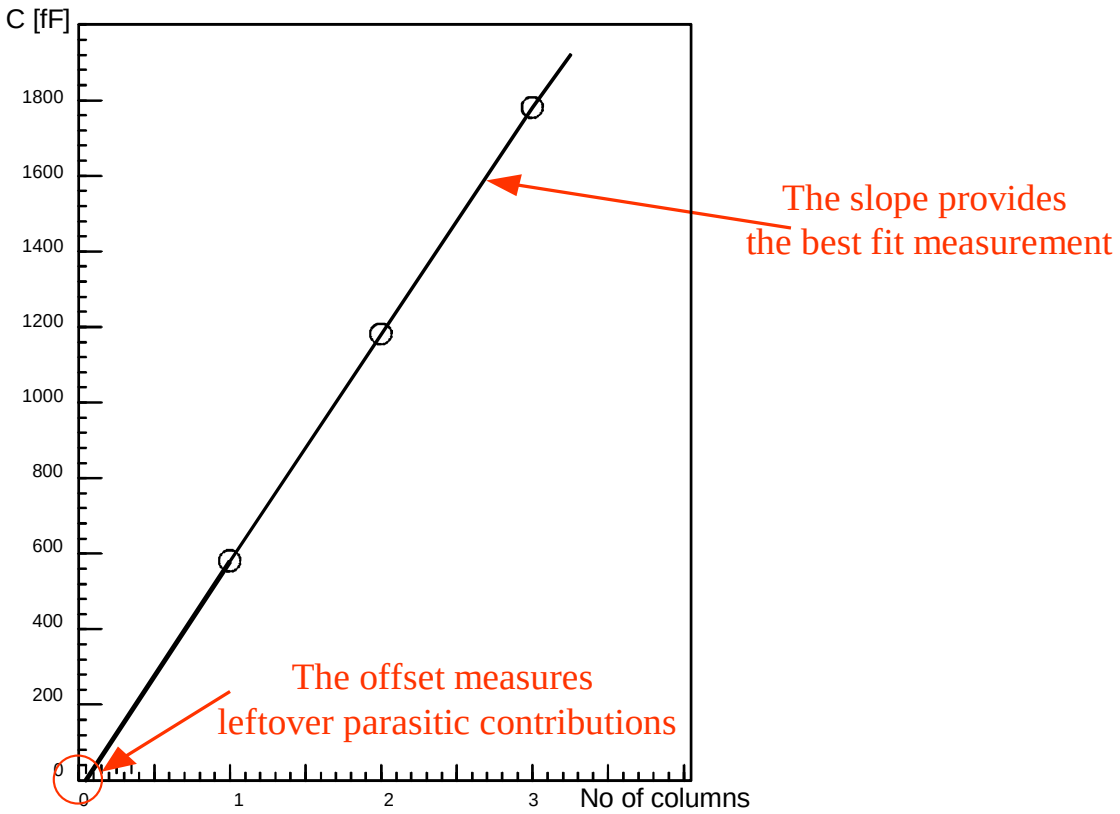
- assign the boundary conditions:
  - 1 V on the central pixel
  - 0 V on the other pixels of the array & backplane

  => C_ip and C_diag numerically equals to the charge on the nearest and diagonal neighbour

- define a mesh and let the Laplace equation be solved by a Finite Element method (140 K elements and 150 K nodes for the 7x7 pixel array)



For each structure , redundancy and internal consistency has been provided isolating 3 bias columns of pixels, so that capacitances for 3 single columns, 3 doublets and 1 triplet were measured



Capacitance offset[fF]				
	Chip1	**Chip 2**	**Chip 5**	**Chip 6**
Implant width/ pitch [μm]	**34/50**	**60/100**	**50/75**	**100/150**
Offset	**-100**	**-7**	**-12**	**-10**

Backplane capacitance [fF]

	Chip1	Chip 5	Chip 2	Chip 6
Implant width/ pitch [μm]	34/50	50/75	60/100	100/150
Measured by the CV curves	185 ± 5	218 ± 5	368 ± 5	447 ± 5
Measured as (C_ip+C_bkpl)-C_ip	314 ± 35	160 ± 45	391± 51	376 ± 40
TOSCA simulation	211 ± 60	233 ± 35	412 ± 90	466 ± 70
TOSCA Single pixel	0.8 ± 0.2	1.9 ± 0.7	3.2 ± 0.7	7.3 ± 1.1

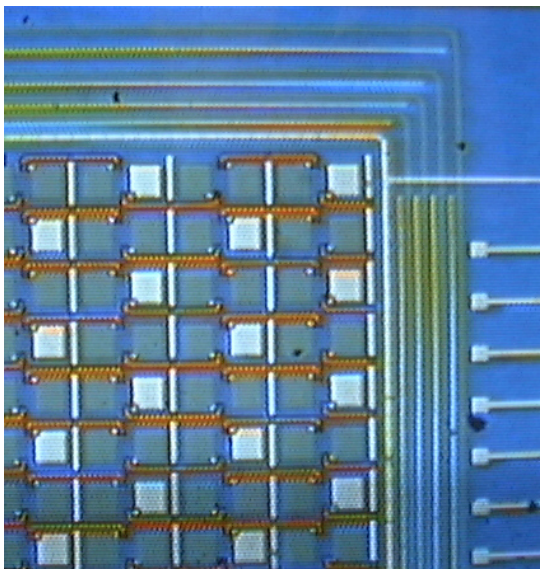
- sum of all of the pixels along 1 bias line
- simulation results for the single pixel

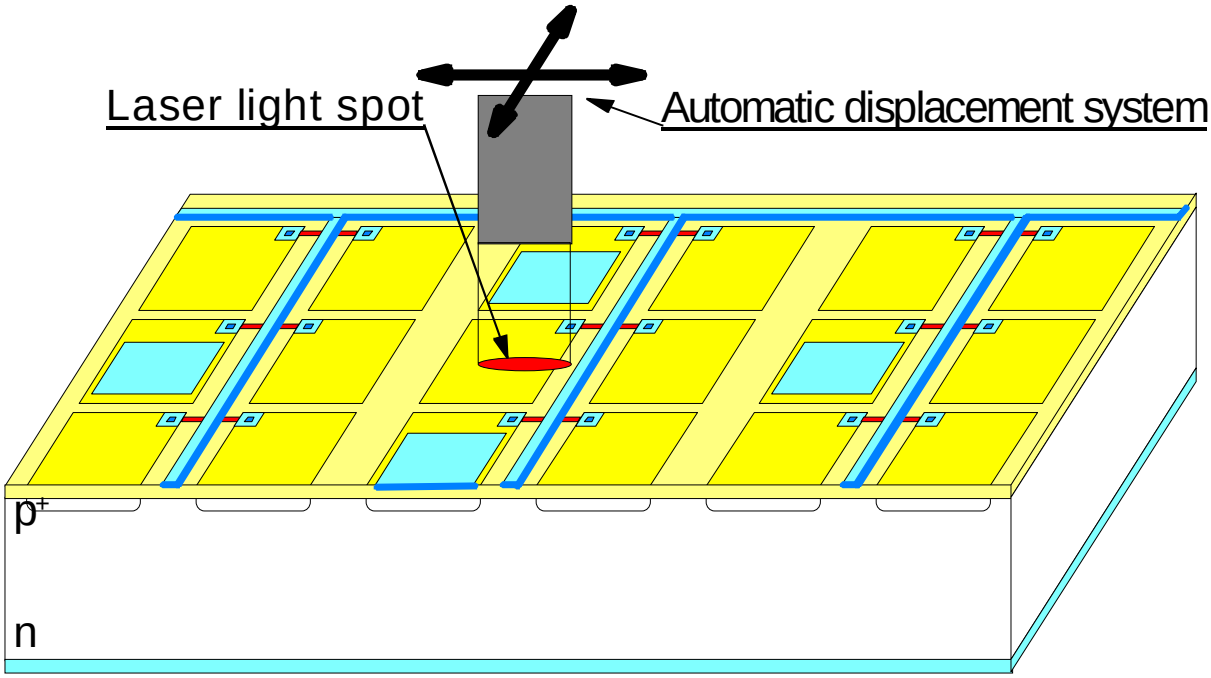
Interpixel capacitance [fF]

	Chip1	Chip 5	Chip 2	Chip 6
Implant width/ pitch [μm]	34/50	50/75	60/100	100/150
Measured	2098 ± 30	958 ± 5	1038 ± 11	599 ± 5
TOSCA simulation	980 ± 40	690 ± 70	880 ± 67	630 ± 60
TOSCA Single pixel nearest neigb. Ci	1.3 ± 0.2	1.8 ± 0.1	1.9 ± 0.1	3.7 ± 0.1
TOSCA Single pixel Total Ci tot	8.6 ± 0.4	11.8 ± 0.6	12.7 ± 0.6	22.3 ±1.1
TOSCA Single pixel backplane C	0.8 ± 0.2	1.9 ± 0.7	3.2 ± 0.7	7.3 ± 1.1

- sum of all of the pixels along 1 bias line
- simulation results for the single pixel

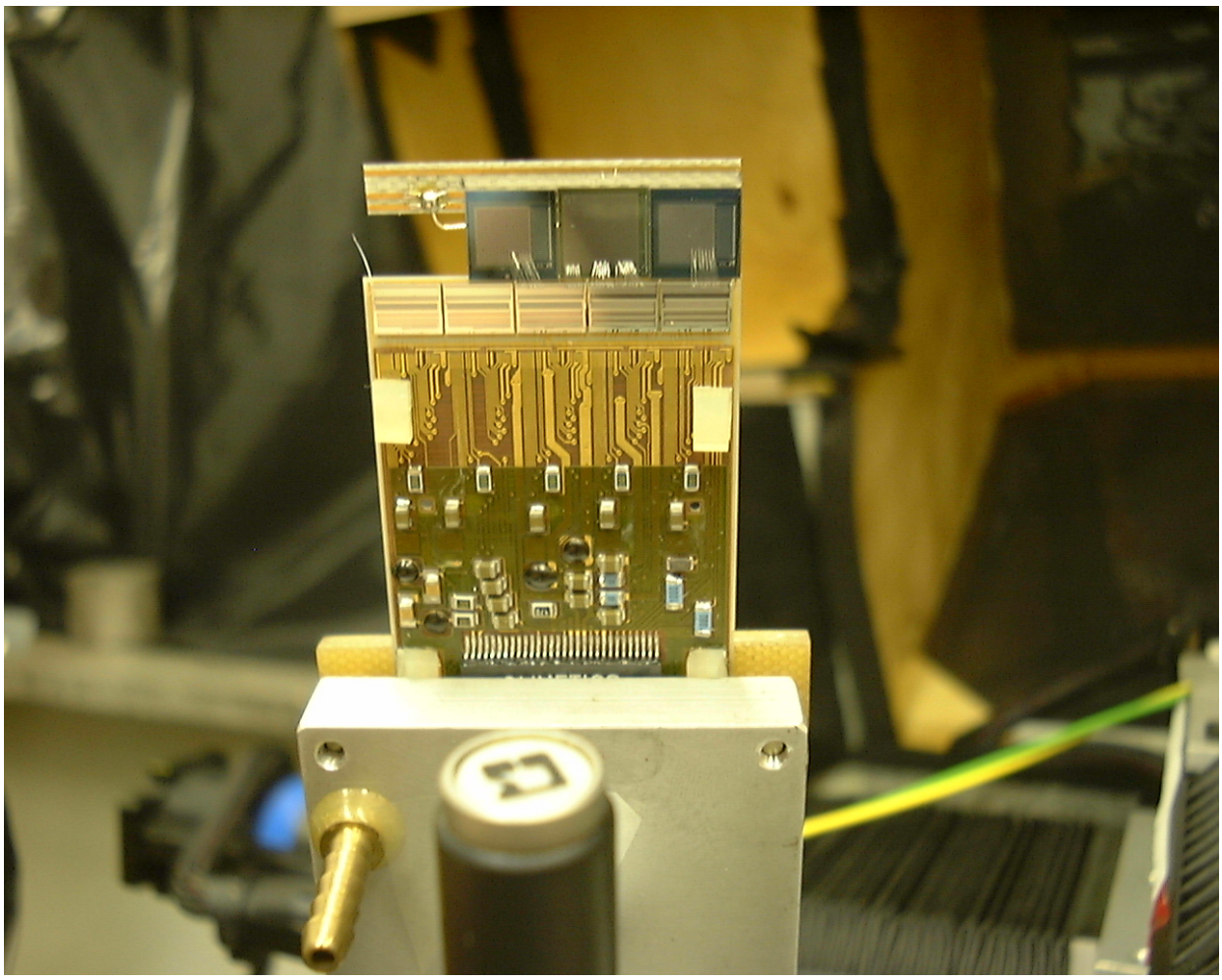
Charge collection study on a structure with 100 μm pitch and implant width 60 μm





An infrared diode of 880 nm wavelength was used, shining on the BACKPLANE – the penetration depth is ~ 10 μm

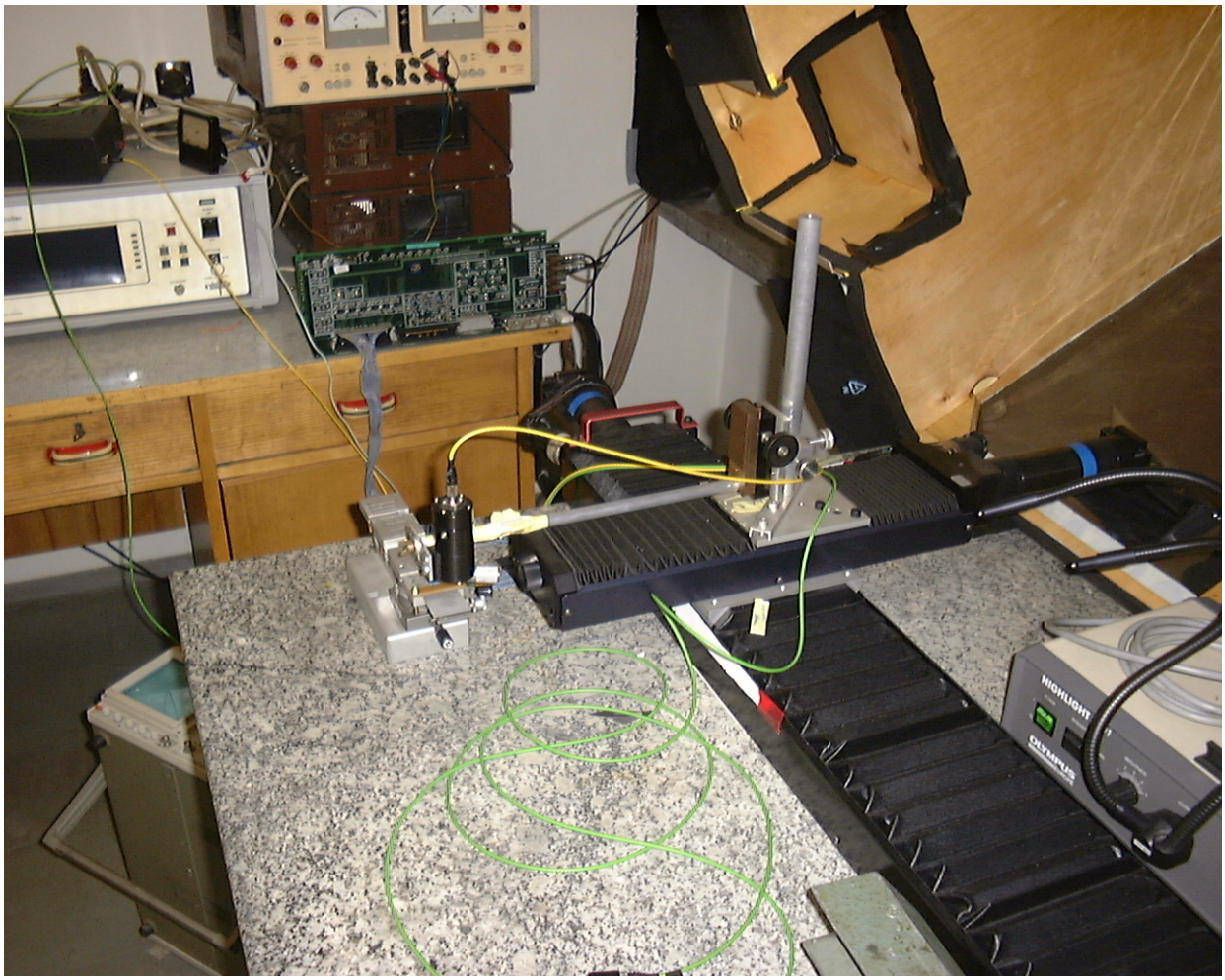
Set up



The read-out pixels were wire bonded to the readout electronics chip.

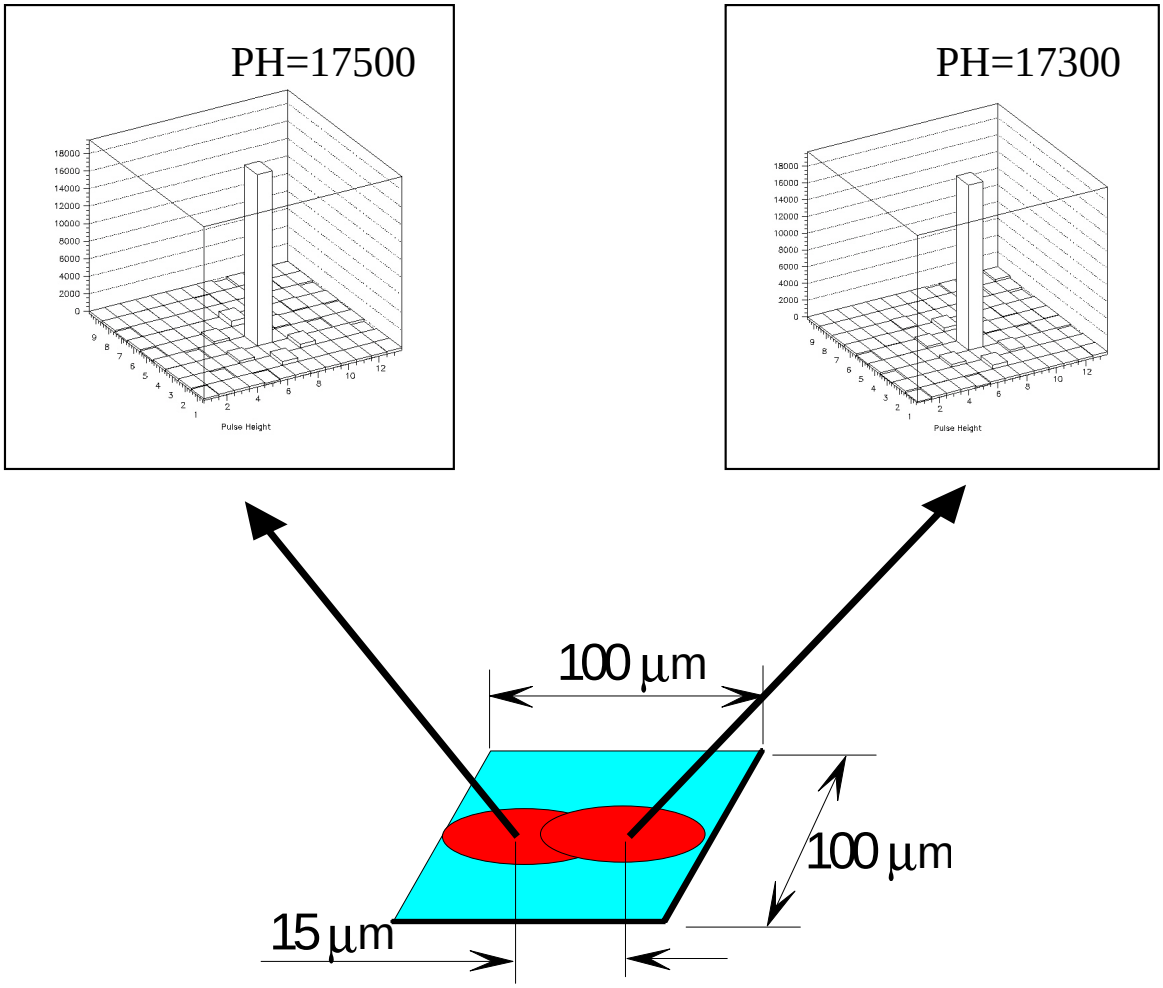
The BELLE experiment amplifiers and readout chain were used

Measurement Setup



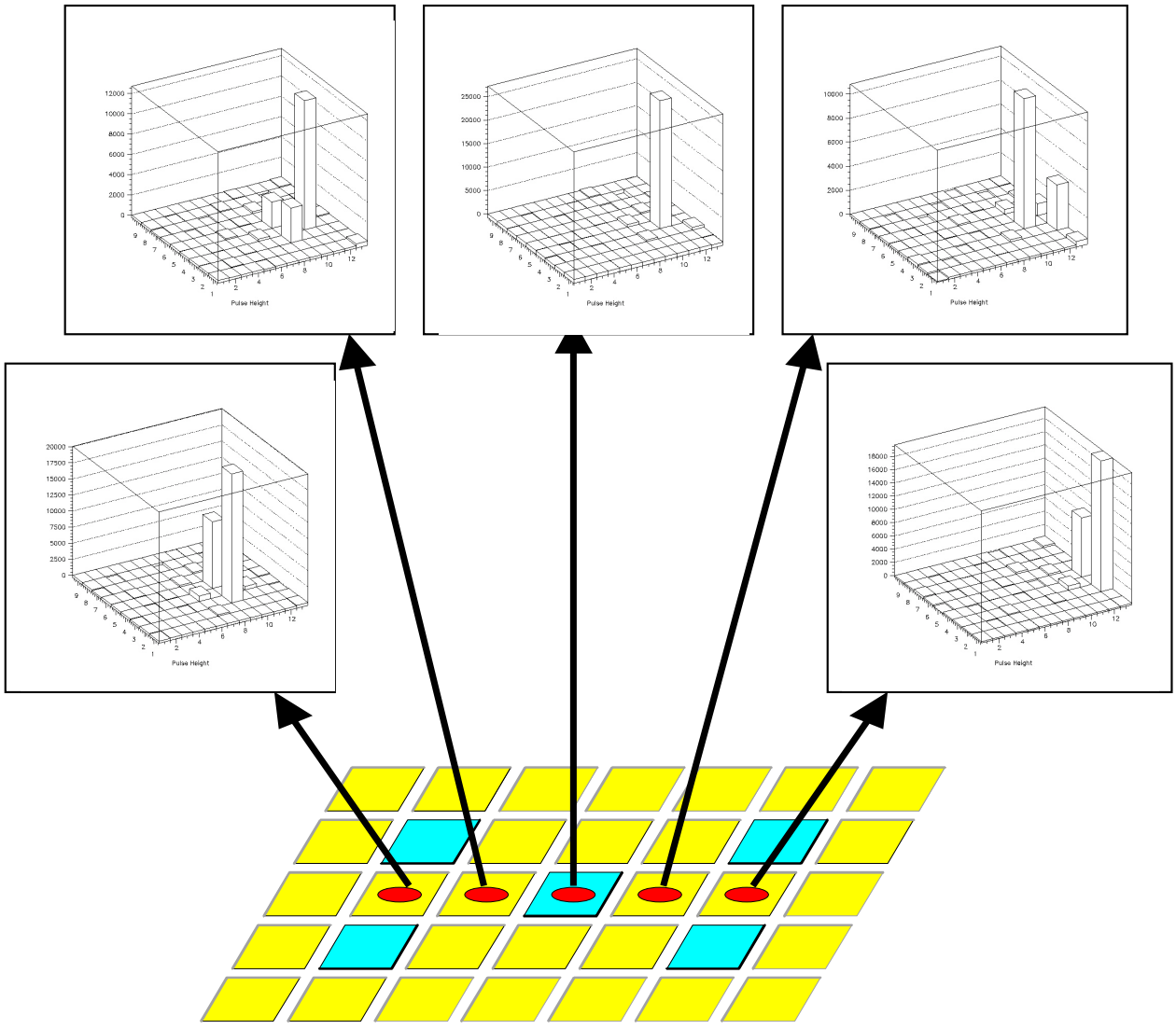
X axis with 1 μm precision movement
Y axis with 10 μm precision movement

Estimation of Laser Spot Size



The laser spot size was below 85 μm

Capacitive Charge Division

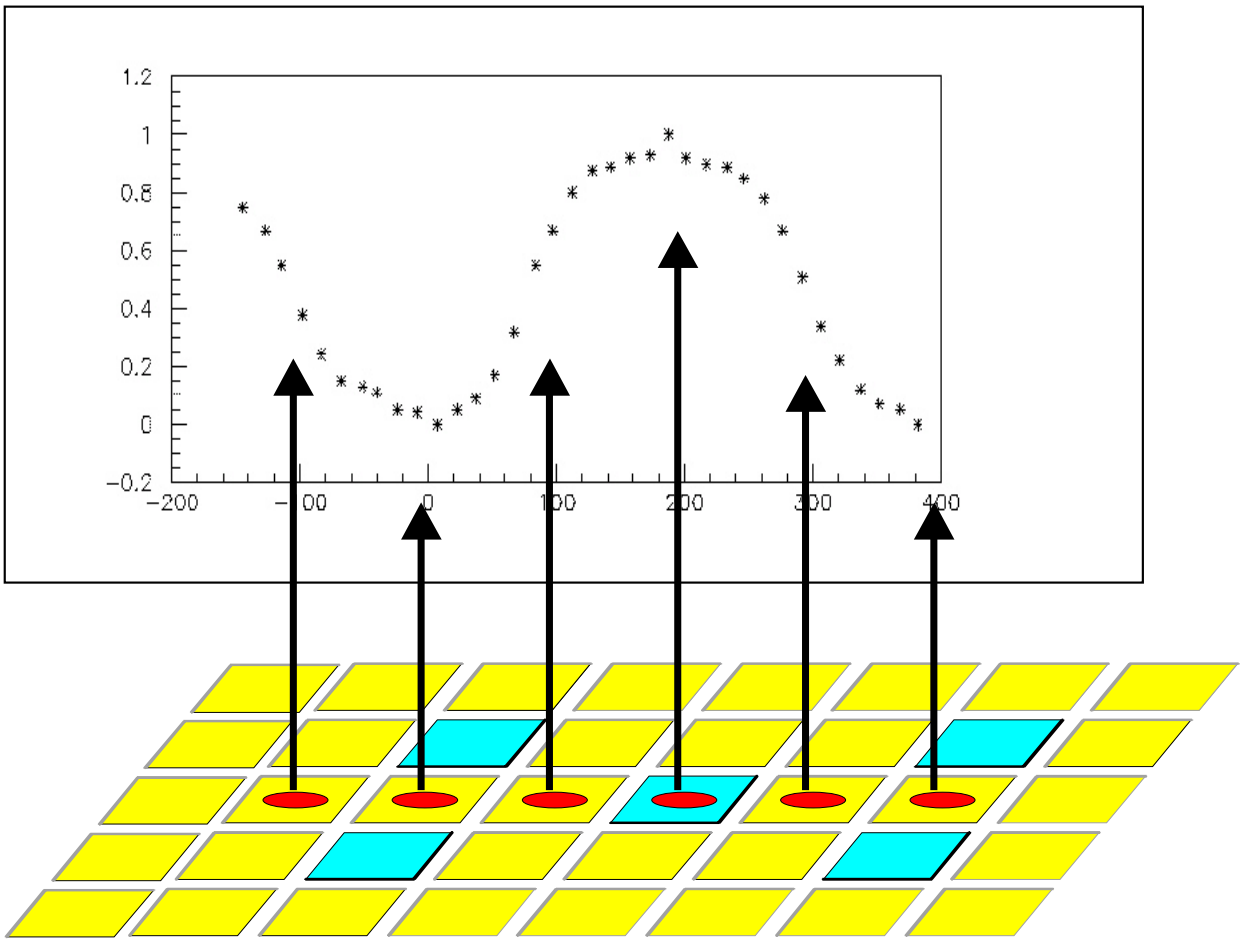


The IR spot was moved across the detector and ~ 100 event were recorded for each position

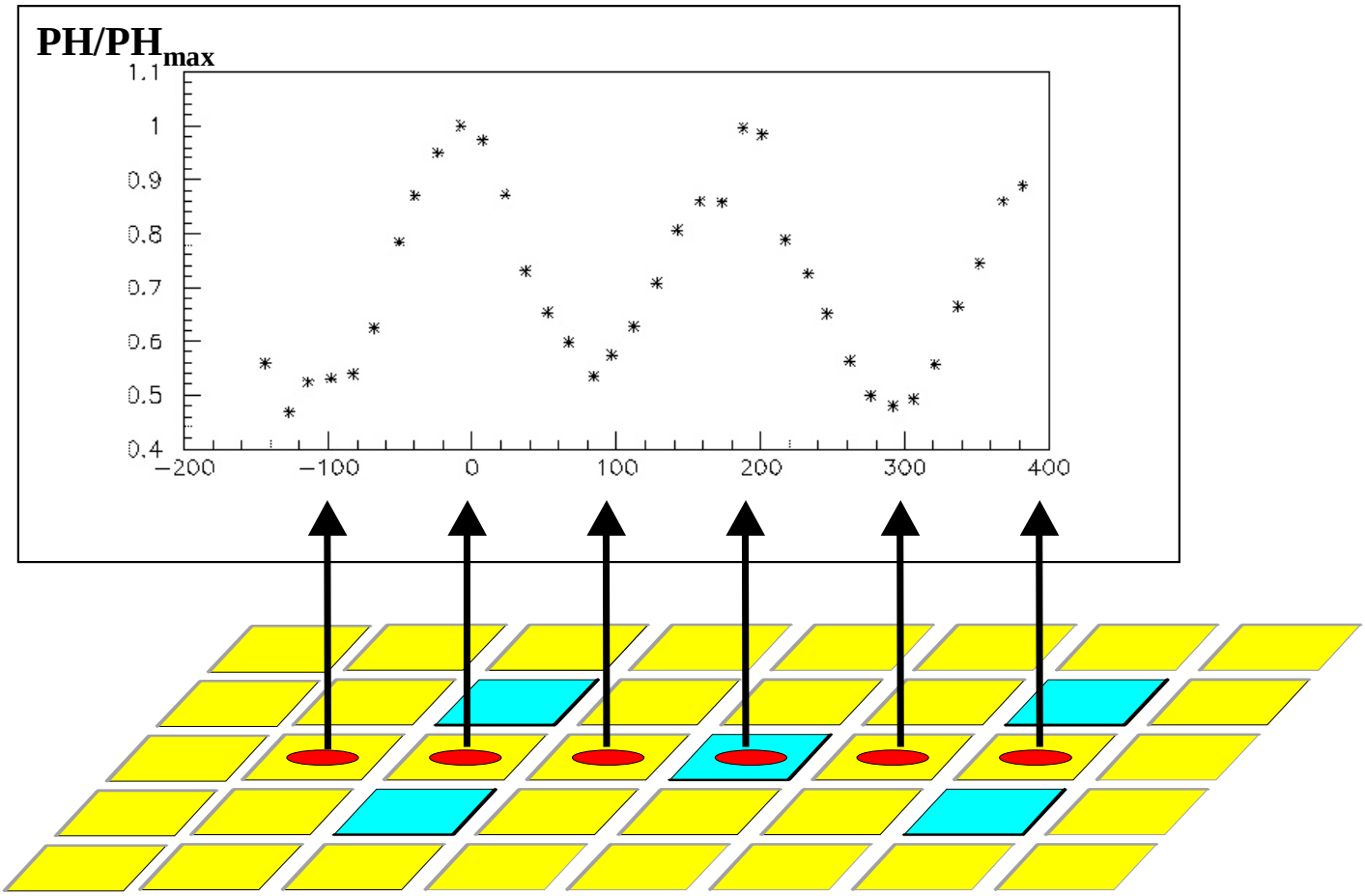
Charge sharing

$\eta = PH1/\Sigma PHn$

where n depends of the number
of nearest neighbors n=(3, 4, 5)

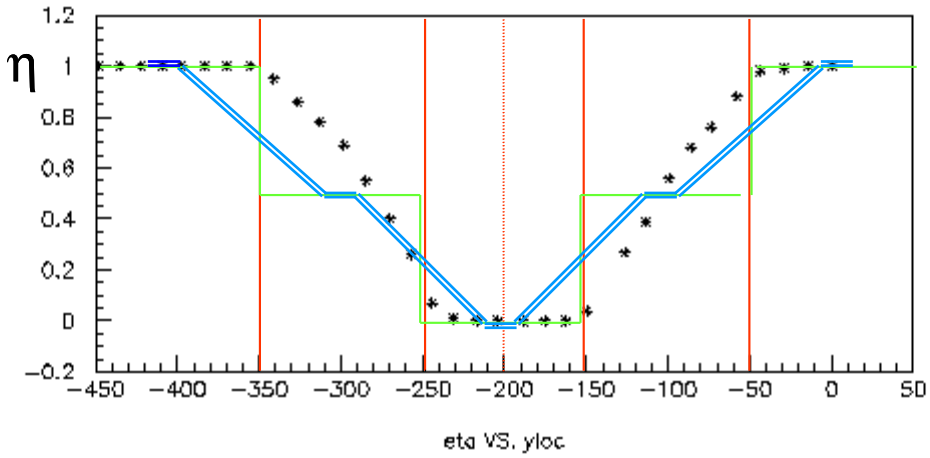


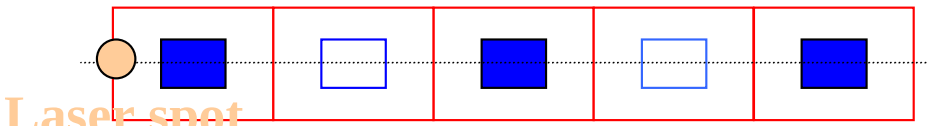
Cluster Pulse Height



The measured charge loss matches what is expected by a network analysis based on the measured interpixel and backplane capacitances

Charge sharing II





Laser spot

Read out pixels

Interleaved pixels

NO diffusion, capacitive coupling only

Diffusion and capacitive coupling with a 25 μm pitch

Resolution < 25 μm/√12

Conclusions

• A prototype pixel detector with interleaved pixel has been designed and fabricated

•

• The technological quality of the prototypes is satisfactory

•

• The electrostatics characterization proves the reliability of the design

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• Preliminary IR laser tests on one of the prototypes proves the efficiency of the charge sharing mechanism

•

• Exhaustive charge collection measurements on a short timescale are planned

•

• A second round aiming for

a/ 25 micron pitch

b/ improved testing capabilities

c/ compatibility with existing pixel readout chips

d/ enhanced interpixel capacitance

are planned on a 1 year timescale, together with test beam for resolution measurements