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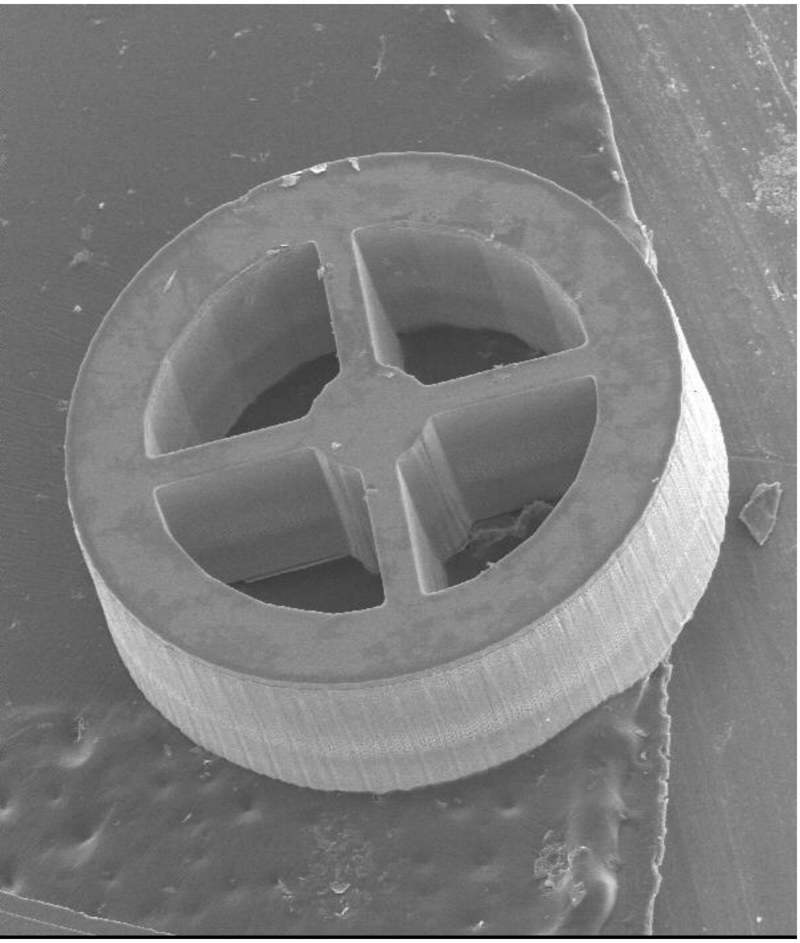
LCWS2000, Fermilab, Oct 25

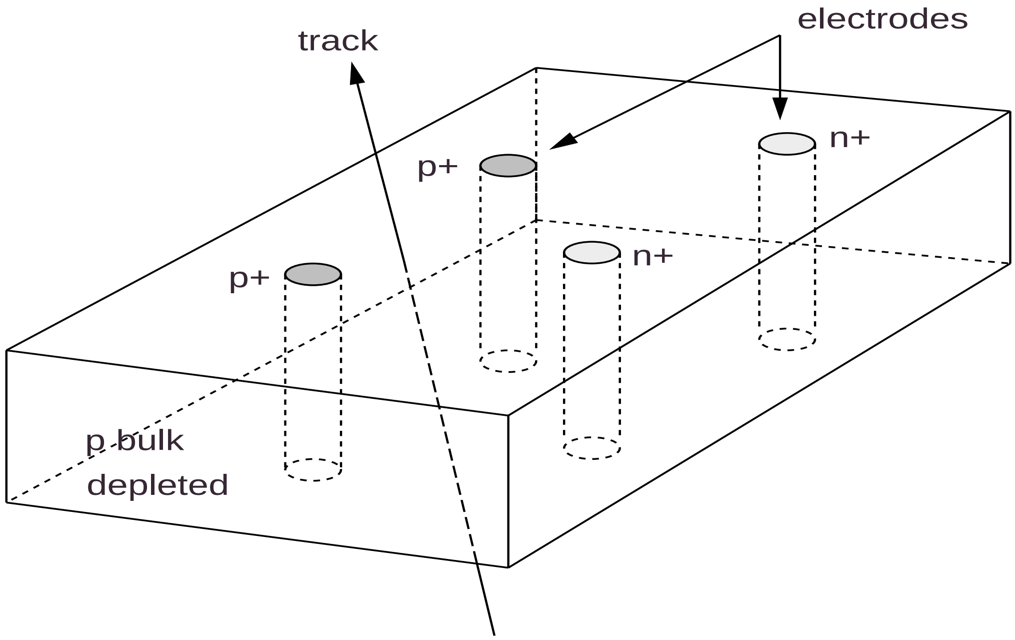
Pixel detector R&D @UH

- 3D sensor development
  - Good timing
  - Low depletion voltage
  - Active edge
- Small footprint electronics
  - 40X60 µm or 50X50 µm
- Bump bonding
  - IR inspection of bonded chips

Enabling Technology

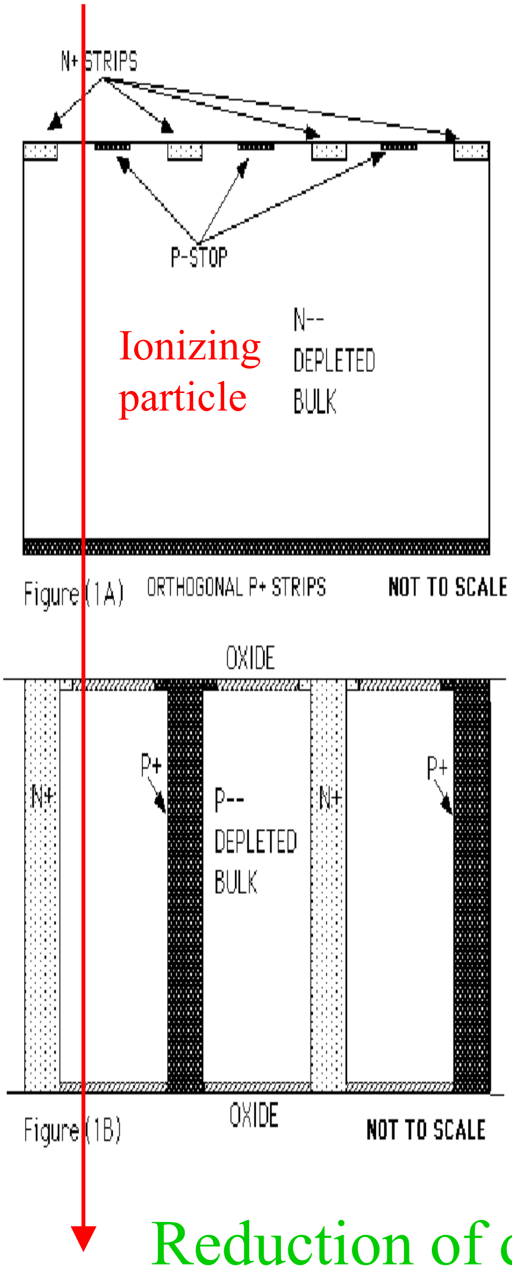


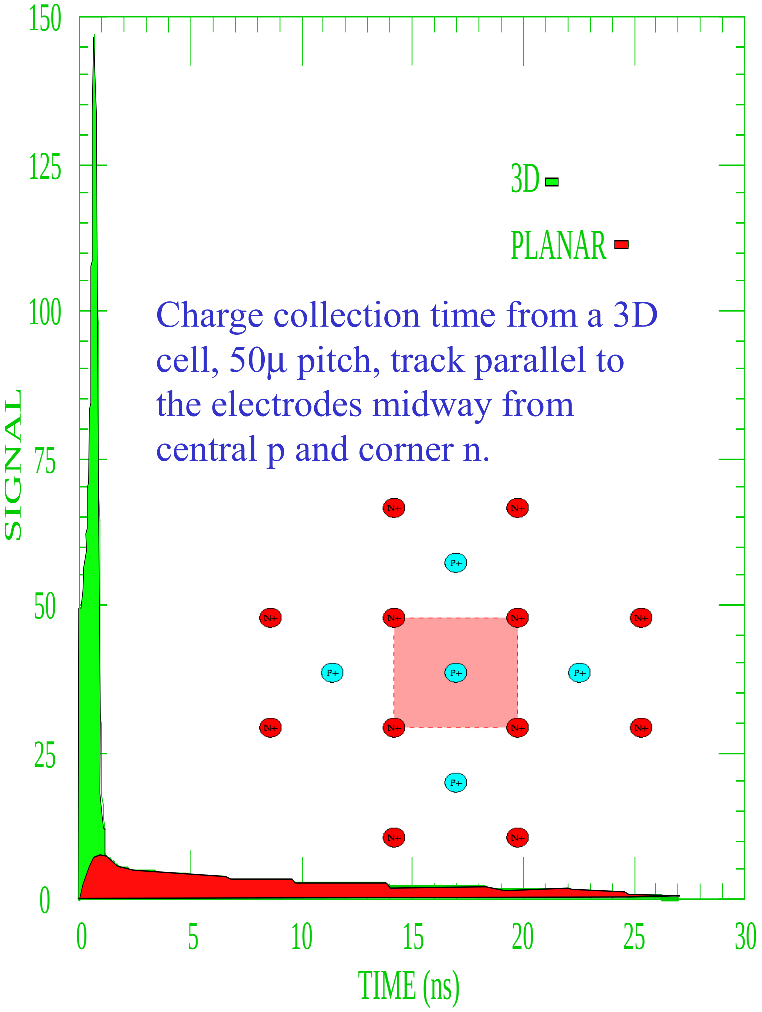
- Can now etch deep, near-vertical holes with plasma technology @STS
- With low pressure and moderate temperature process, a conformal coat of polysilicon is formed
- Dopant gasses can be added to the silane and make p^+ and n^+ doped polysilicon
- Heating drives the dopants into the surrounding silicon forming the p-n junction



Detector Development

Good timing!





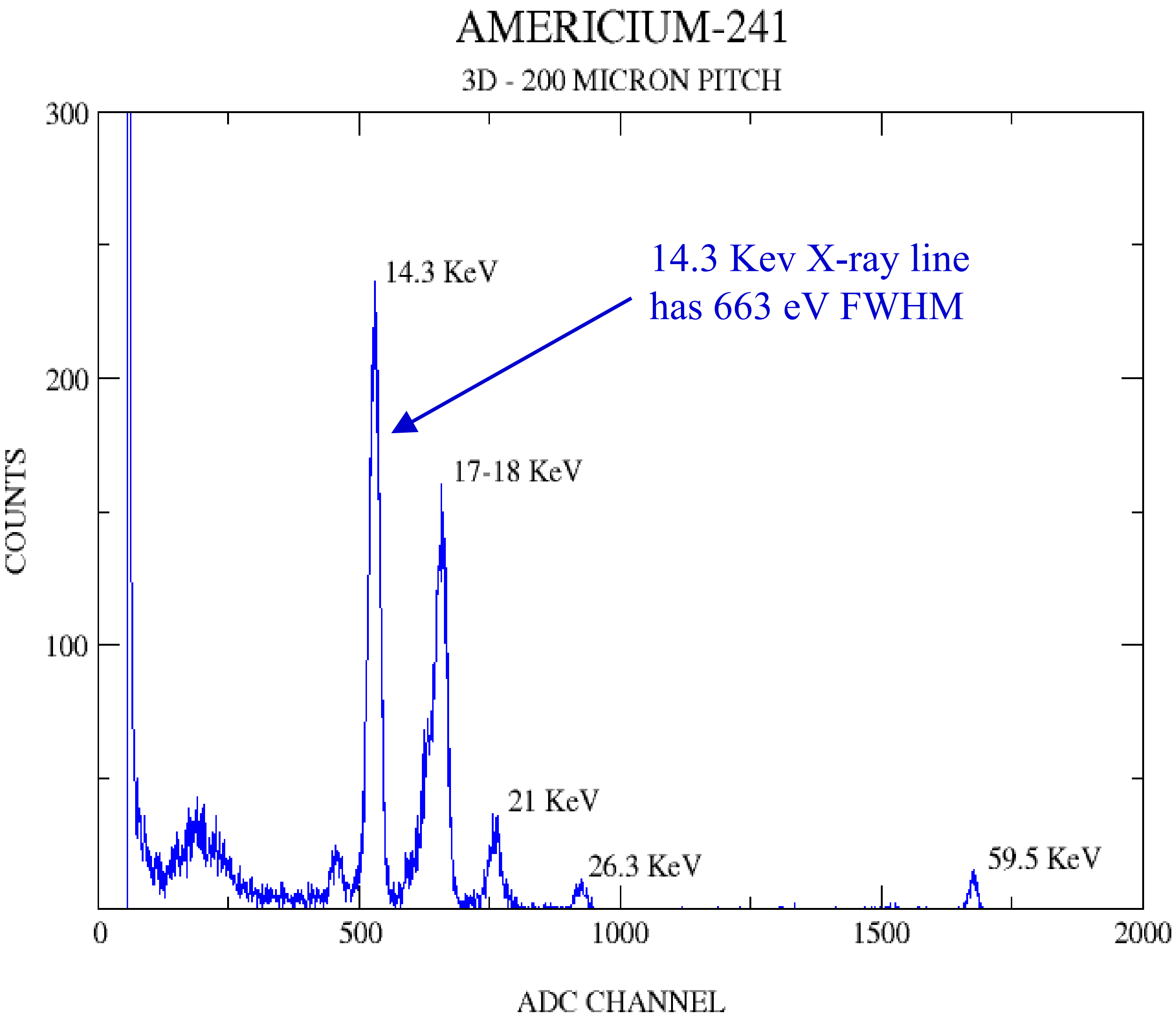
Charge collection time from a 3D cell, 50µ pitch, track parallel to the electrodes midway from central p and corner n.

Reduction of distance between electrodes:

- Reduction of drift time
- Reduction of depletion voltage

Detector Results - sensitivity

- Charge sensitive amp, 1 µsec shaping time
- "Strip detector" with 14 P-type electrodes tied
- 200 micron pitch strip to strip, 100 micron between electrodes within a strip

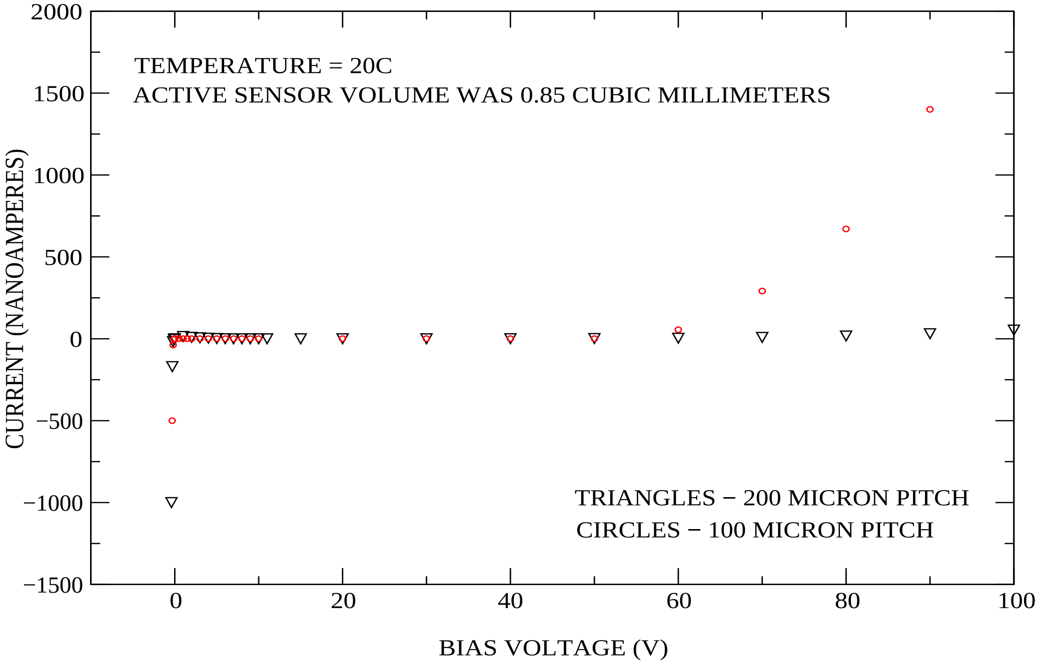


14.3 Kev X-ray line has 663 eV FWHM

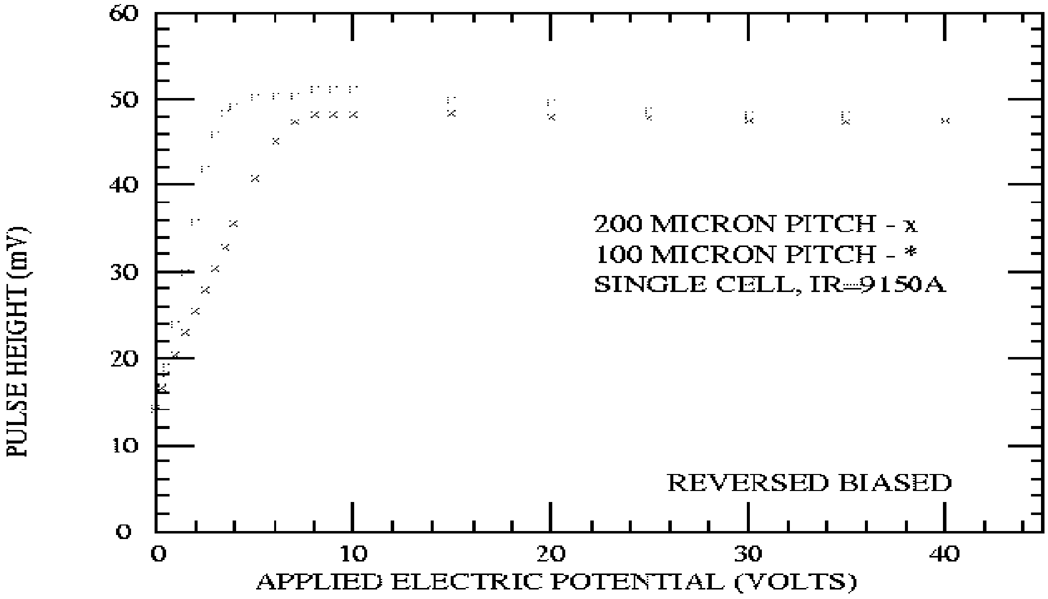
Detector Results

Reasonable leakage current and

Low depletion voltage: 5-10 V

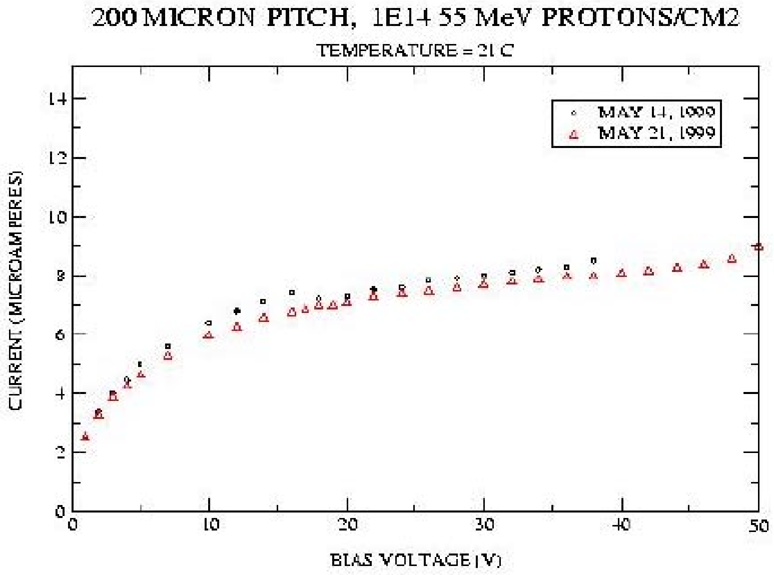


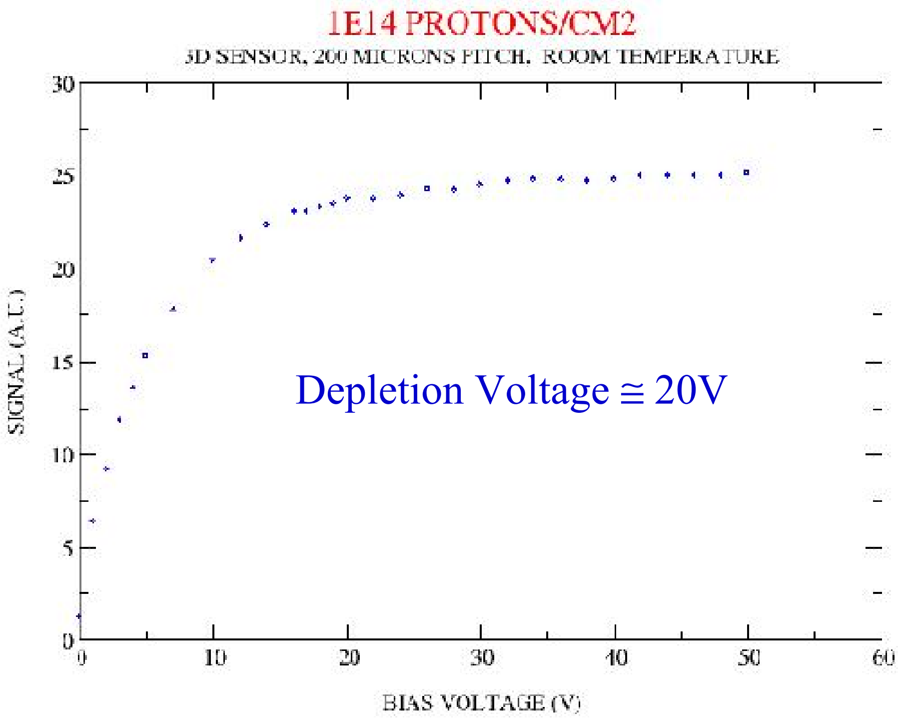
LEAKAGE CURRENT



Radiation Tests

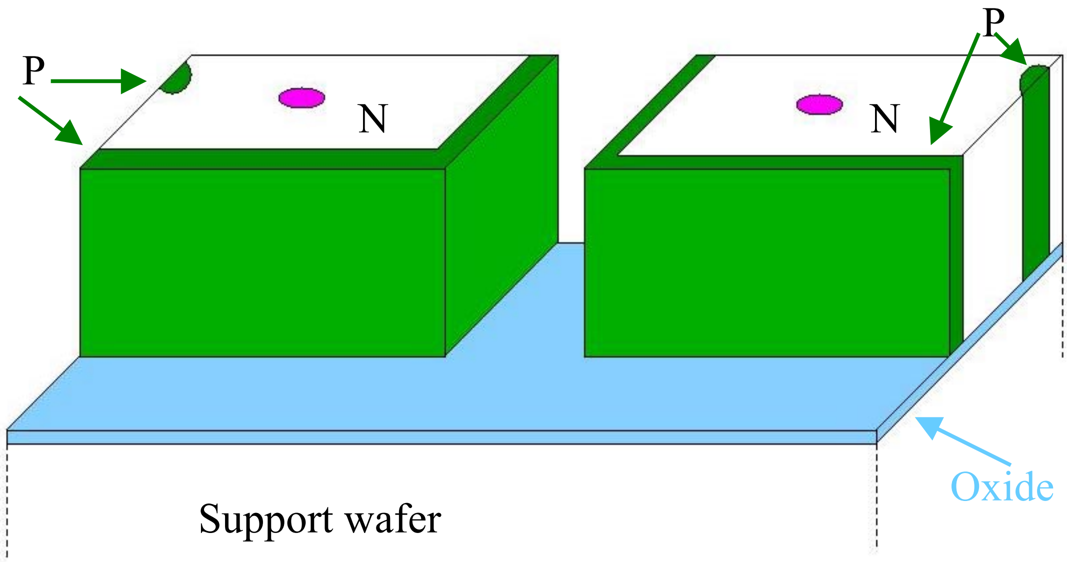
FOR 1 x 10^{14} 55 MeV PROTONS/CM^2





Depletion Voltage ≅ 20V

Active edge



Sensitive up to very edge, no dead area

- Fusion bond to support wafer
- Plasma etch peripheral trench
- Diffuse dopant into exposed single crystal silicon
- Deposit poly, oxide, etc…
- Contact edge with aluminum

Devices behave as diodes with low leakage current

Signal plateau at expected voltage

Sensitive area extends to trench edge

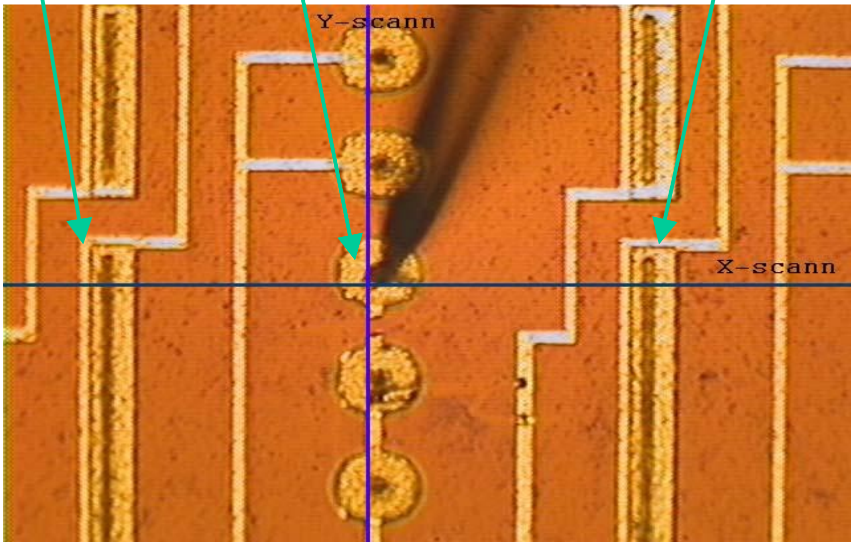
Active edge IR test

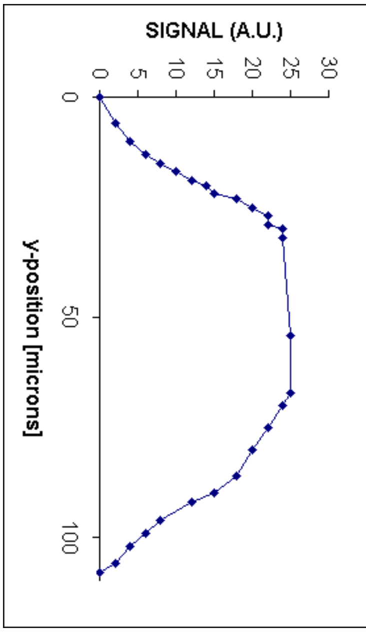
IR peak at 820 nm with full width of 30 µm

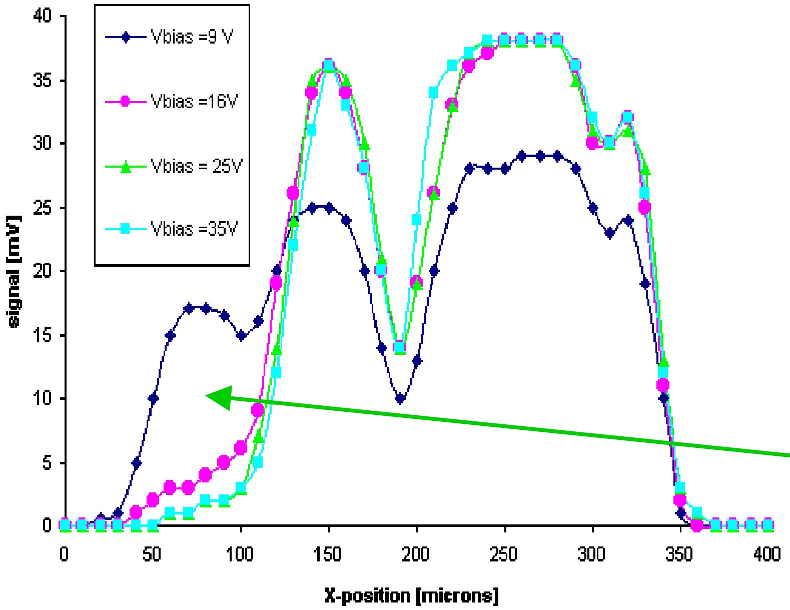
N-trench

Isolated P electrode
connected to a pico-probe

N-trench







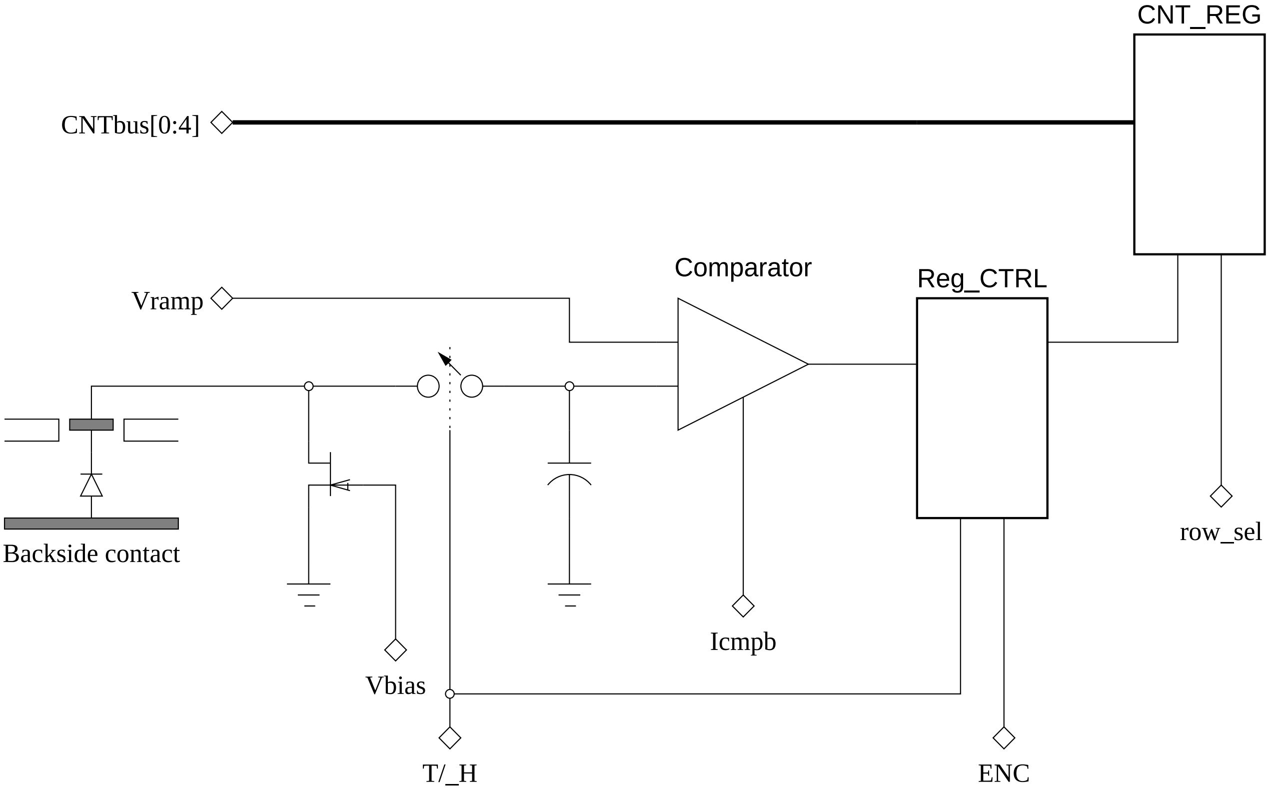
The FWHM of the Y scan is 73 microns, compatible with the 75 microns pitch

The FWHM of X scan is 287 microns, close to the 290 microns spacing between two N-trenches

Unintentional field-oxide transistor is shown by the decreasing of collected signal from the region between 30 and 100 µm

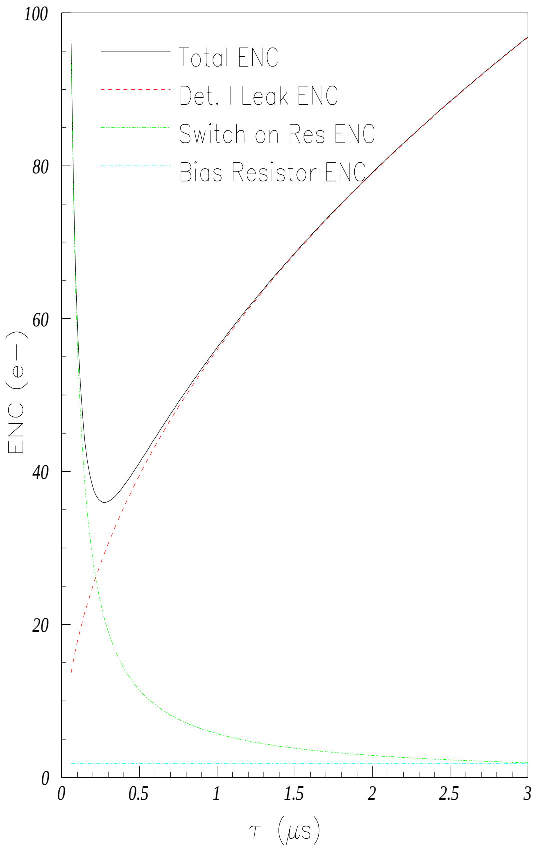
XTEST2 Design

By Gary Varner, UH

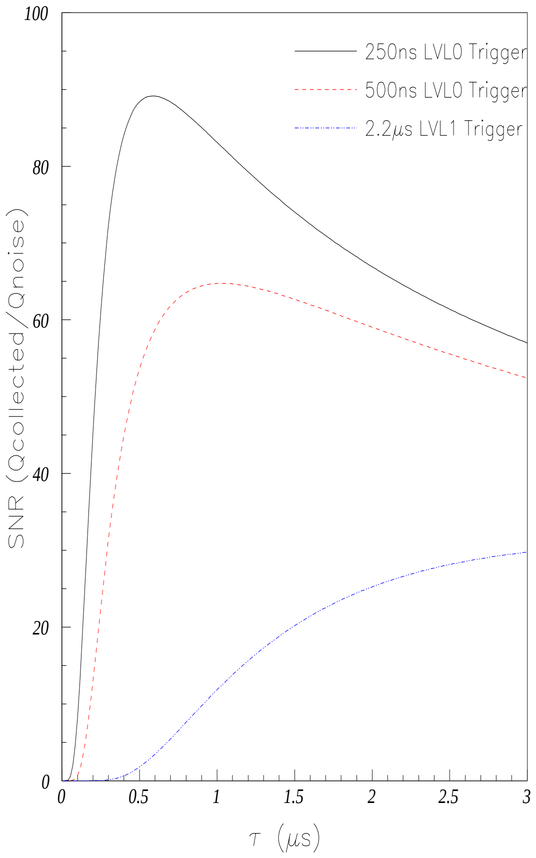


- From 100µm sensor and small Ci, can get a respectably large signal of about 60mV
- Low power comparator convert in “quiet” environment
- After encoding, data ripped out at maximum speed
  - Decent performance w/o pre-amp
  - Comparator powering only during encoding
  - 5-bit Wilkinson encoding takes 40µs
  - After encoding, fast data transfer out in 160µs

Expected Performance



$\tau = R^{eff} \cdot C_{in}$

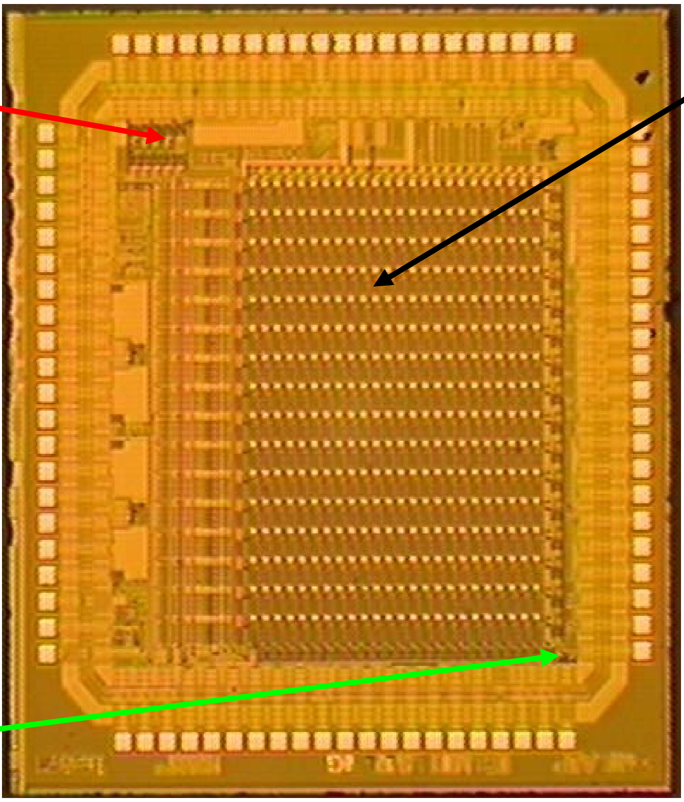


SNR for different trigger time

- Results for 100μm thick sensor

XTEST2 Initial Prototype

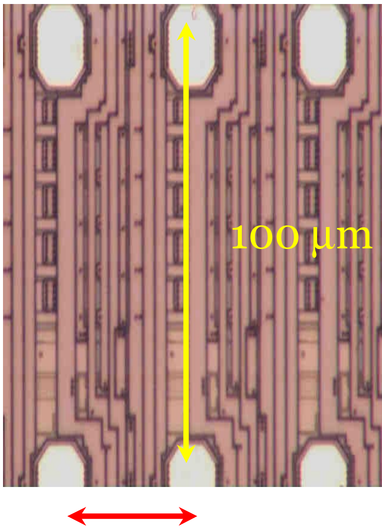
To test feasibility, a prototype (XTEST2) was fabricated in HP 0.5 µm; going to .25 µm technology it is expected to fit in 50X50 µm (or 40X60 µm)



Gray-code Counter

Rad-test structures

16x24 Array of pixels:



50 µm

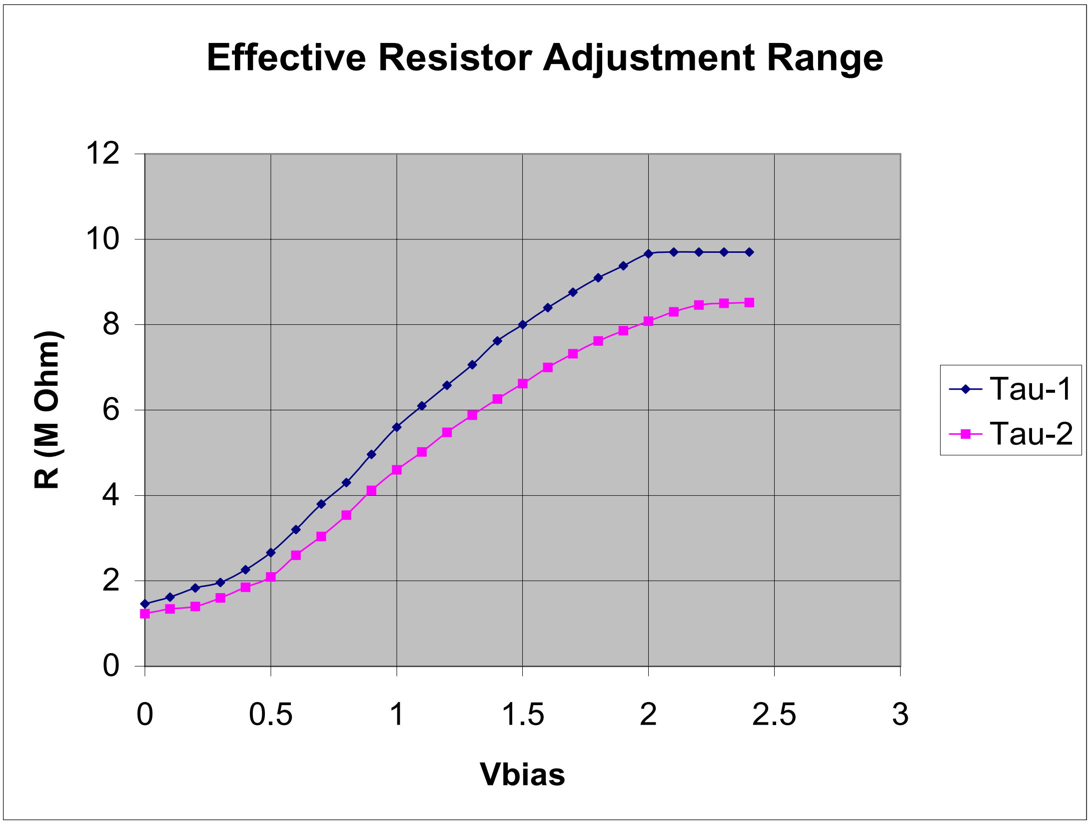
XTEST2 Performance Results

Success:

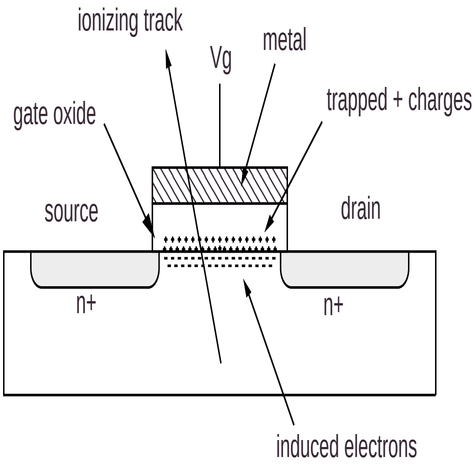
- Comparator works
- Radiation tolerance

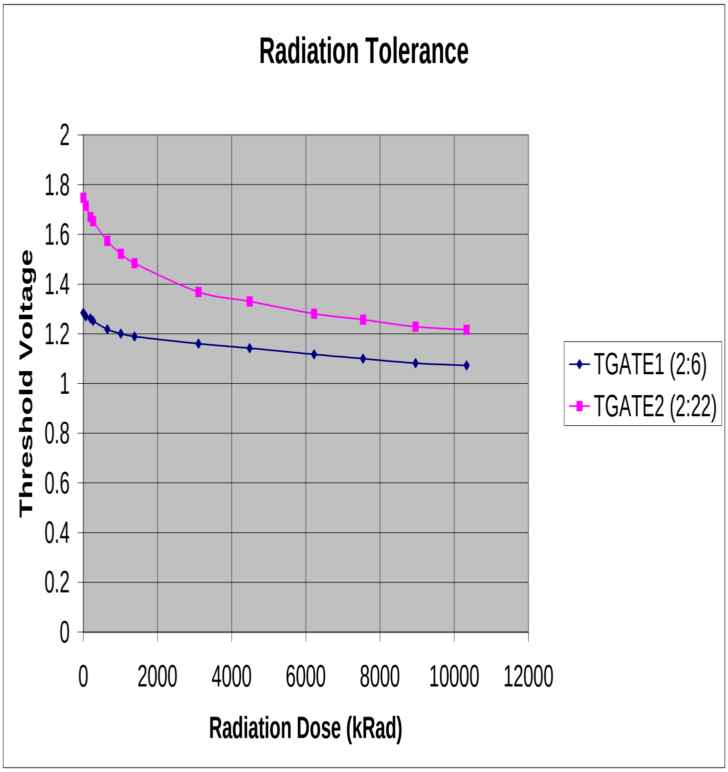
Failures:

- Gray code counter
- Output lines



XTEST2 Radiation Results





Redesigns:

•Better power distribution

•Replace probe pads

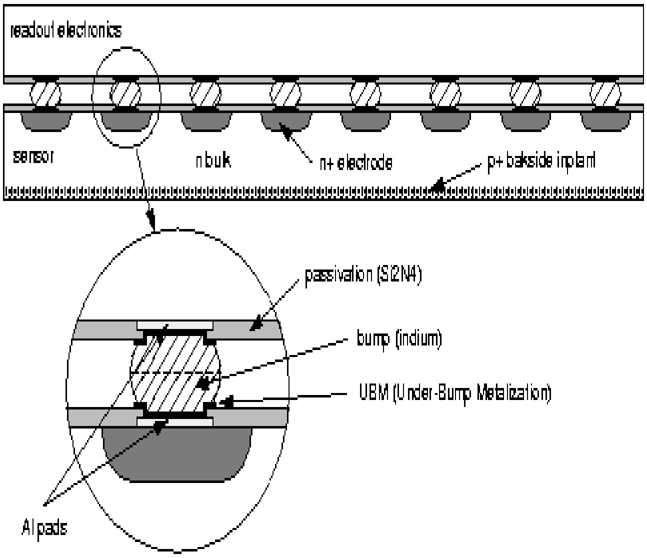
•Clean up wiring

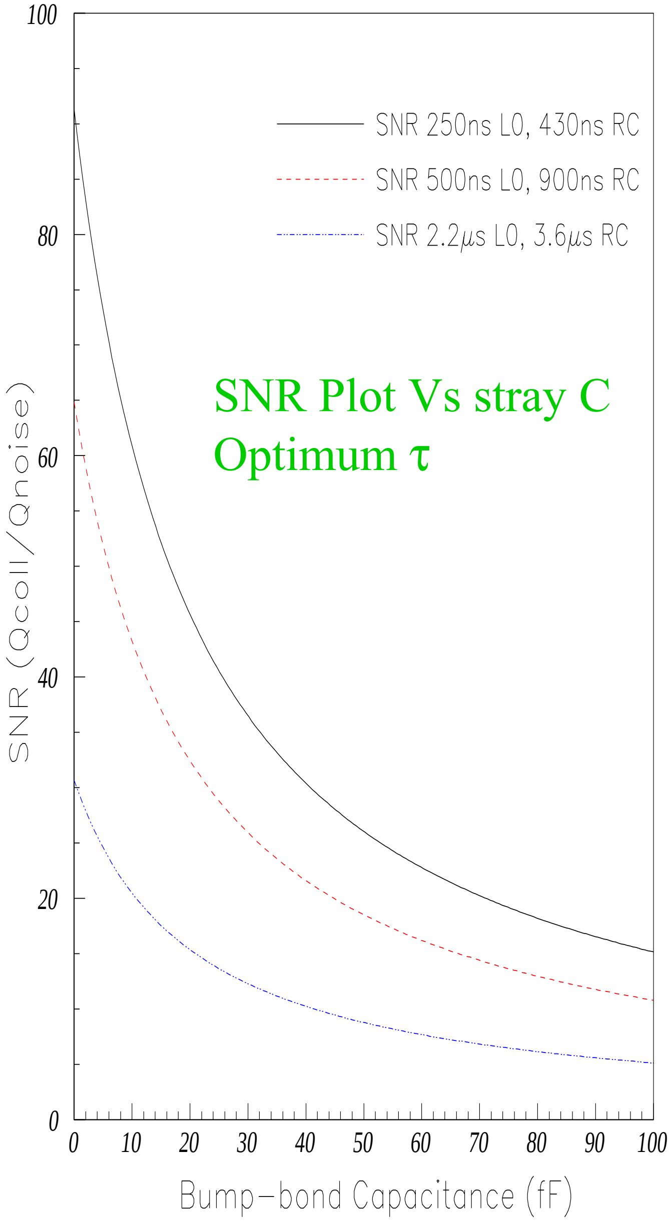
- Radiation hardness
  - Quite adequate total dose performance

Interconnect Concerns

- Excellent SNR and Timing, but…

Assumption all charge is collected is FALSE!





SNR Plot Vs stray C
Optimum τ

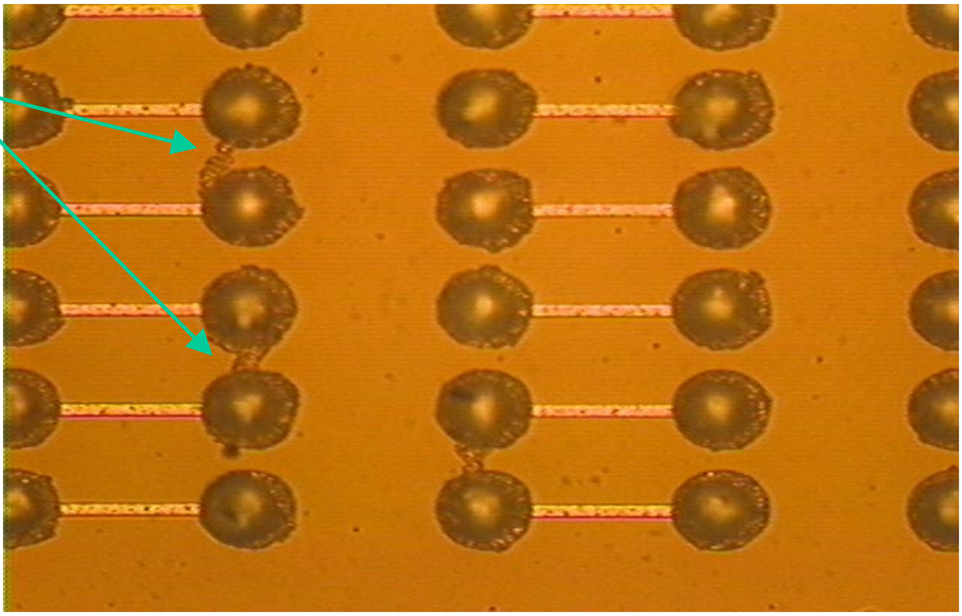
For faster trigger time, even 100fF stray C would yield to SNR about 20.

For larger stray C the degradation may become unacceptable.

Test bumps for real measurement (evaluation from first principles is quite complex)

Bump Bonding Tests

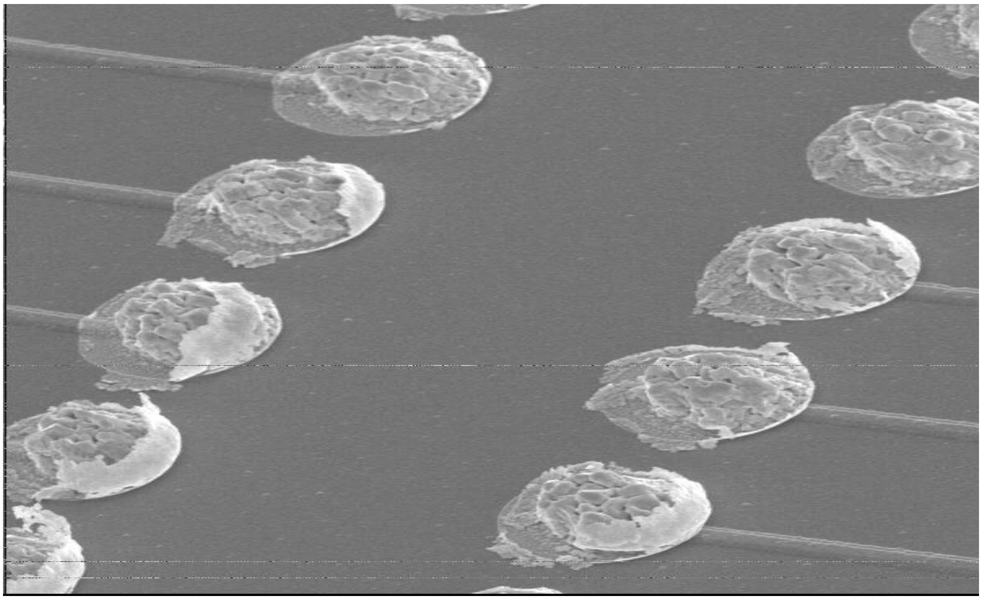
Bonded both 300µm and 100µm thick devices @ AIT Hong Kong.



UBM problems.

Images of unbonded chips

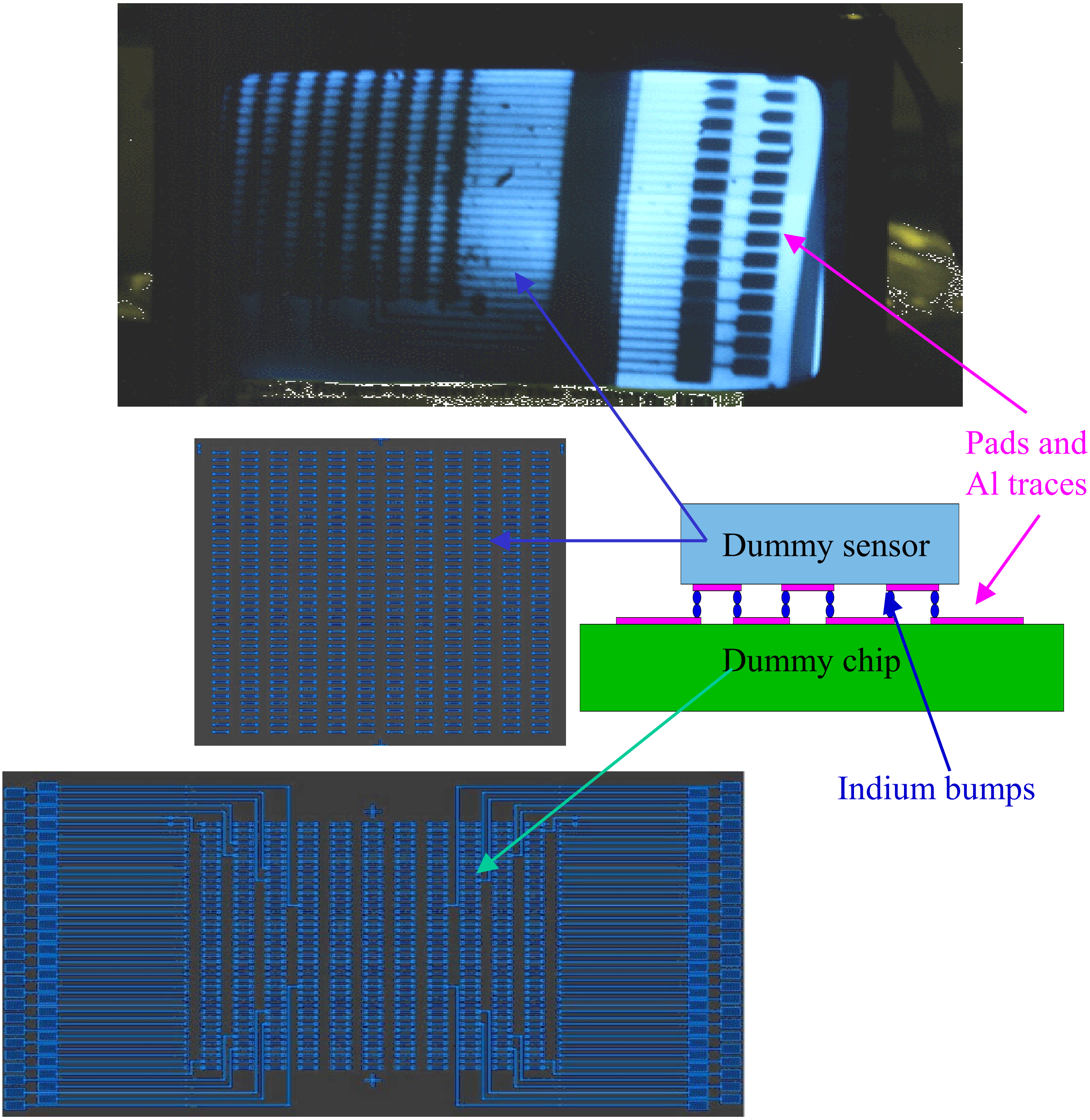
Optical



SEM

IR images

Can examine aluminum traces and In bumps while sandwiched between a pair of bonded chips



Pads and Al traces

Dummy sensor

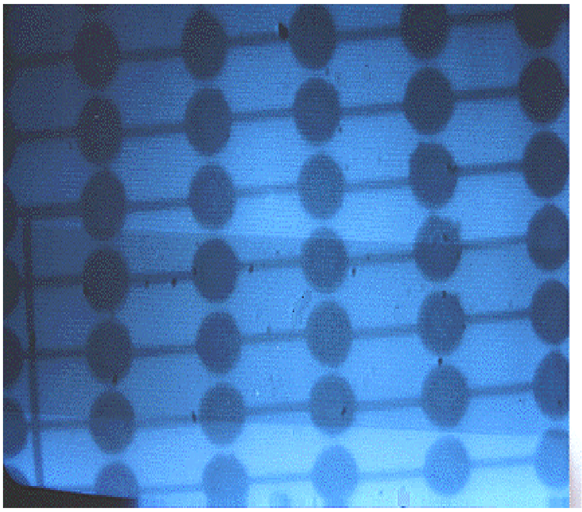
Dummy chip

Indium bumps

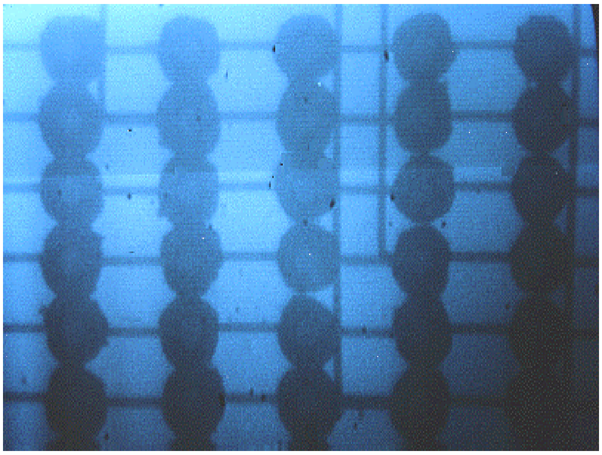
IR analysis

50X100μm pitch bumps

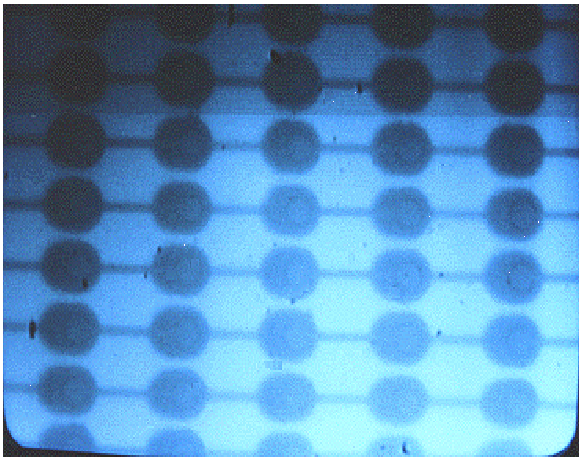
Good!



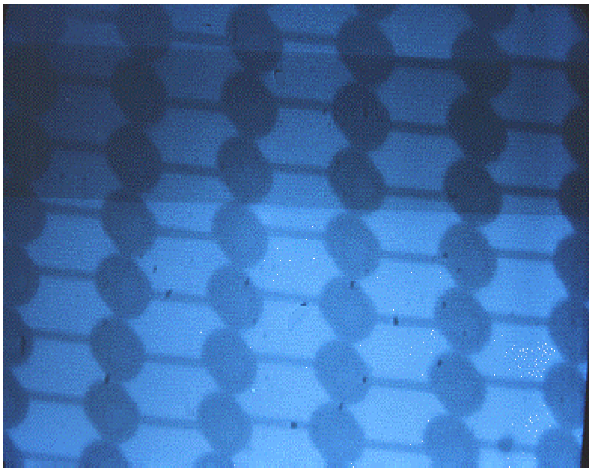
…smashed…



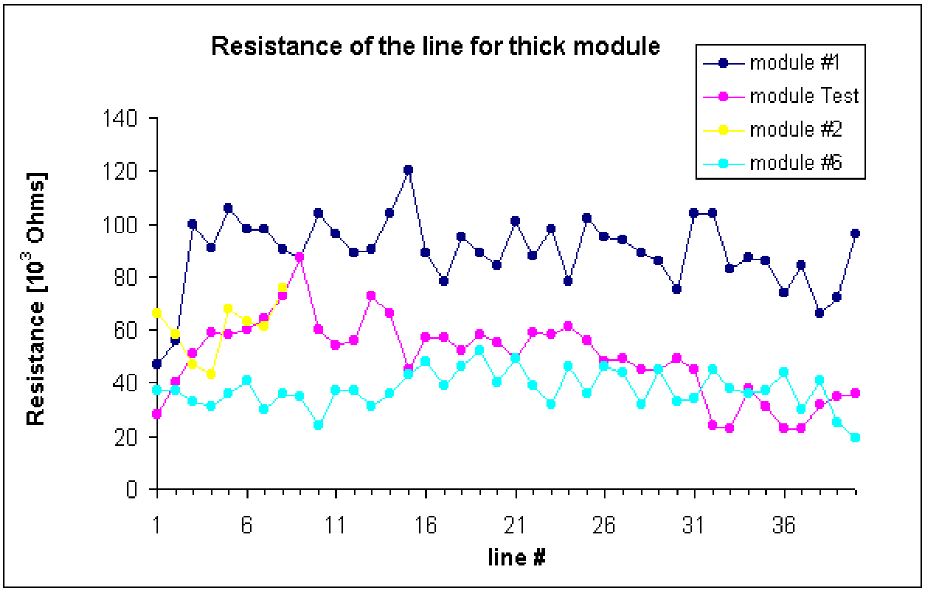
Misaligned…



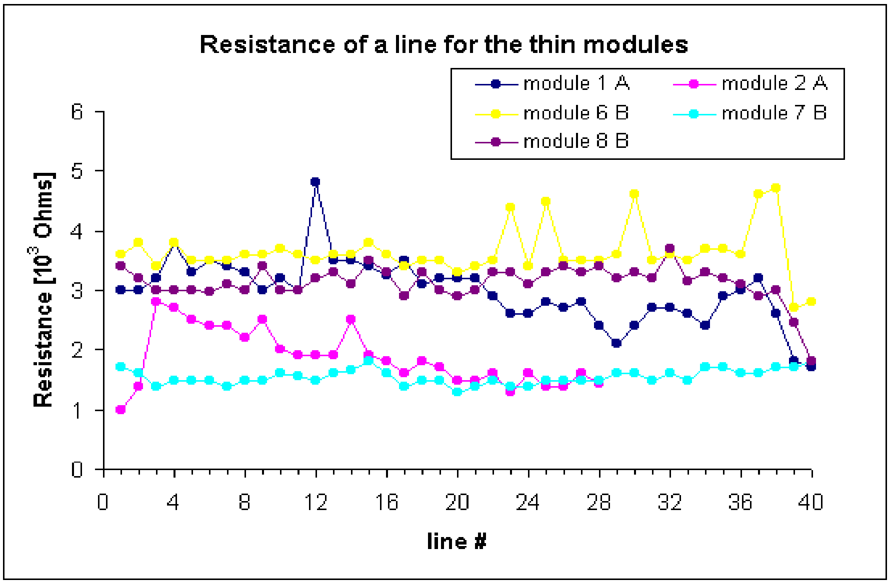
…and misaligned!



Bump bonding Results



- •No open bump-to-bump connection observed out of 21120
- • About 20% of chips bad (learning chips…)
- •Using final "recipe", the remaining 80% had a rate of inter row shorts of about one in a thousand



Conclusions

- First 3D detectors successfully fabricated
  - Reasonable leakage current: 1/4-1 nA/mm^3 at room temperature
  - X-rays and gamma signals have been observed
  - Deplete at low voltages (5-10V) as expected
  - Wide plateau for infrared microbeam signals
  - Preliminary look at active edges promising

- Results from XTEST2 promising:
  - Have established Rad Hard process
  - Developing experience at handling interconnect issues
  - New prototype design submitted by end 2000

- Achieved an acceptable yield bump bonding 100-micron thick sensor and read out chip
- First prototype system mid next year