

# **An electronic system for simulation of neural networks with a micro-second real time constraint**

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## Overview

- Introduction
- Context of the study
- Our System
- Description of the System
- Time Analysis of the System
- Comparizon with Micro-Processors
- Conclusion

## Introduction

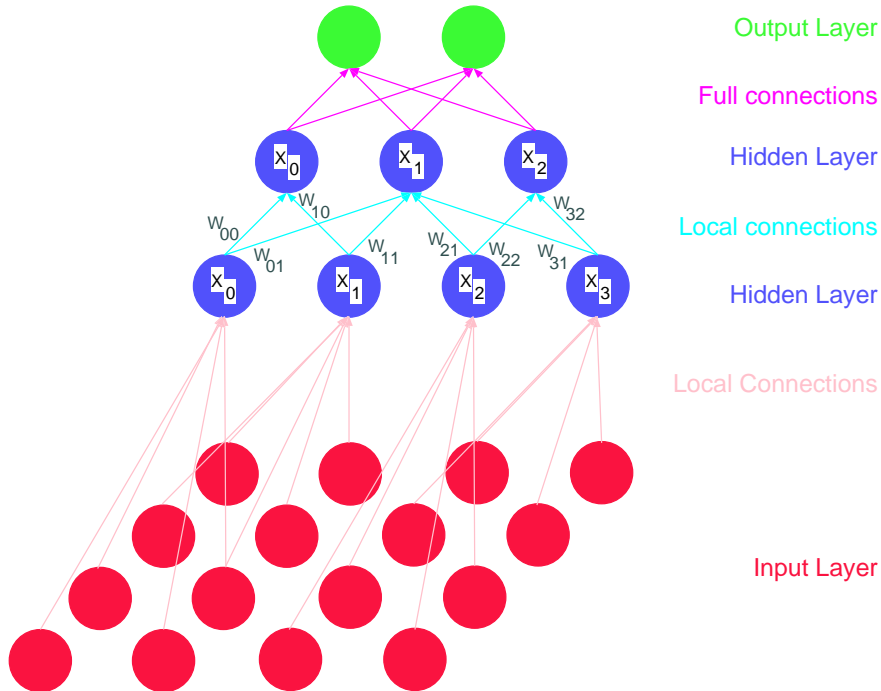
- ☞ We have an electronic system that satisfy :
  - ☞ low power consumption constraints
  - ☞ high input-output bandwidth constraints
  - ☞  $\mu s$  time constraints

## Context of the study

- ☞ Simulate an HEP Multi-Layer Perceptron (H. Abramowicz, G. Dror and al. - Israel)
- ☞ The network has :
  - A four neurons input layer they are  $dx/dz$ ,  $x(z=0)$ ,  $dy/dz$ , and  $y(z=0)$ ,
  - two eight neurons hidden layer
  - a four neurons output layer given  $pt$ ,  $\tan(\phi)$ ,  $\sin(\theta)$ , and  $q$ , the charge
- ☞ The simulation time constraint is  $10\mu s$ .

# Mutli-Layer Perceptron

## Network organization



## Elementary computation

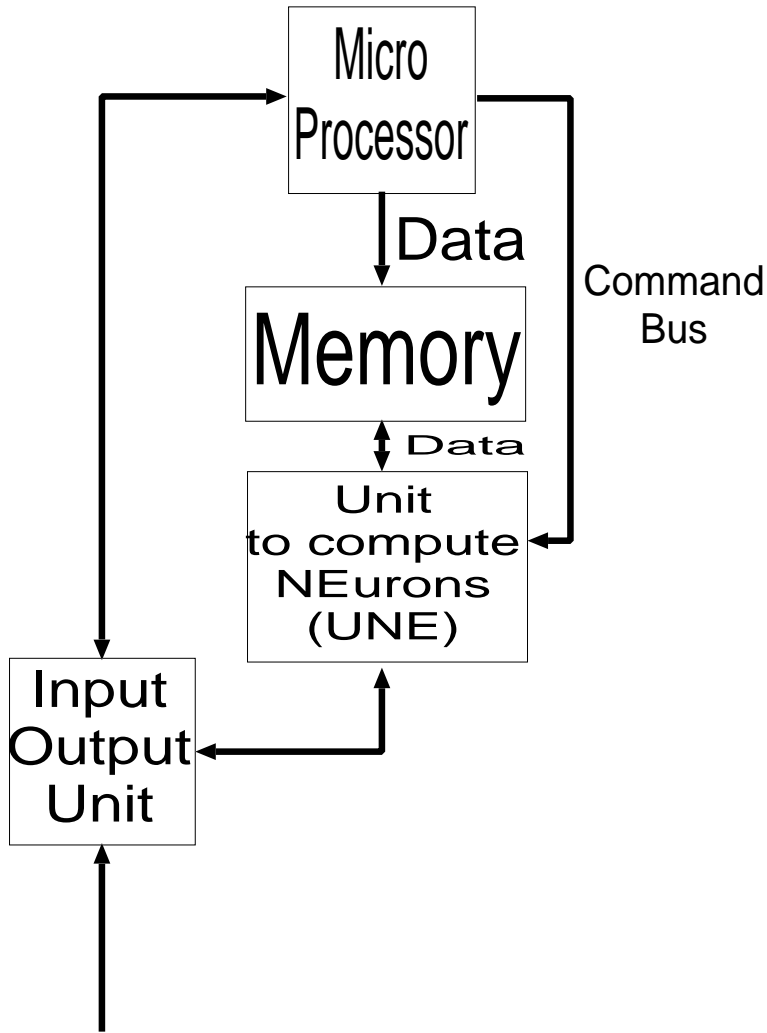
### Post-Synaptic Potential

$$V_i = g \left( X_{j(j \in E_i)} \right) = \sum_{j \in E_i} X_j * W_{ij}$$

### Neuron state

$$X_i = f(V_i) = m \frac{1 - e^{-\lambda V_i}}{1 + e^{-\lambda V_i}}$$

# महाराज्य



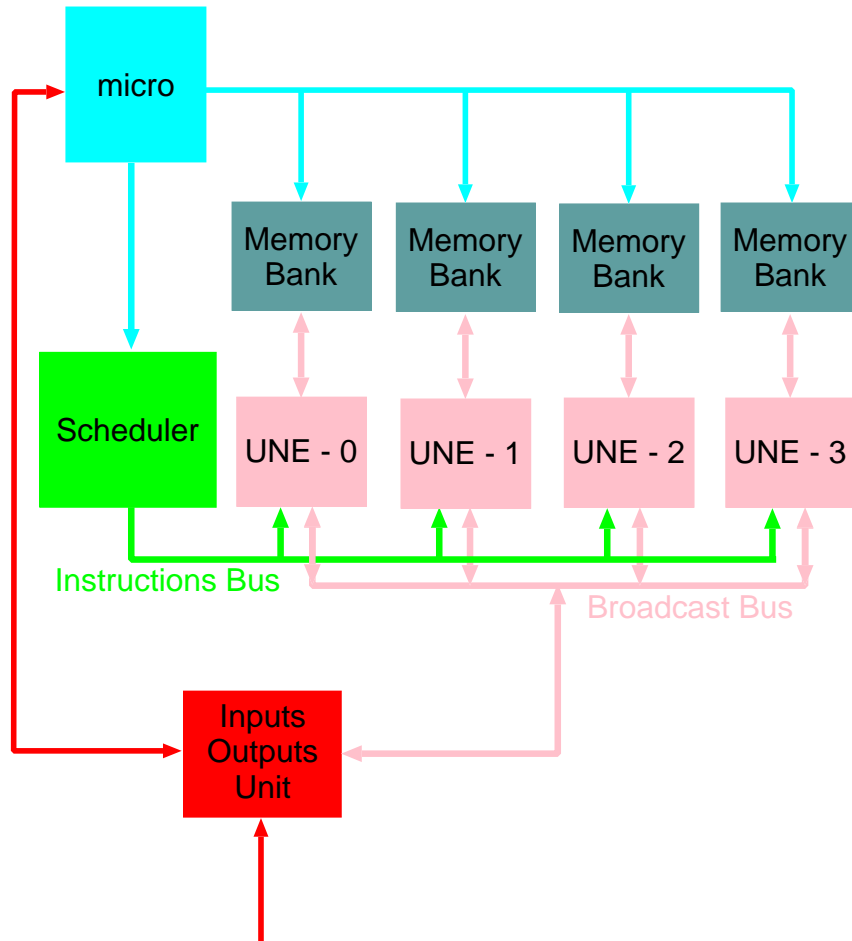
**MicroController** Execution of the sequential part of the algorithm

**UNE** Speedup of the neural computation

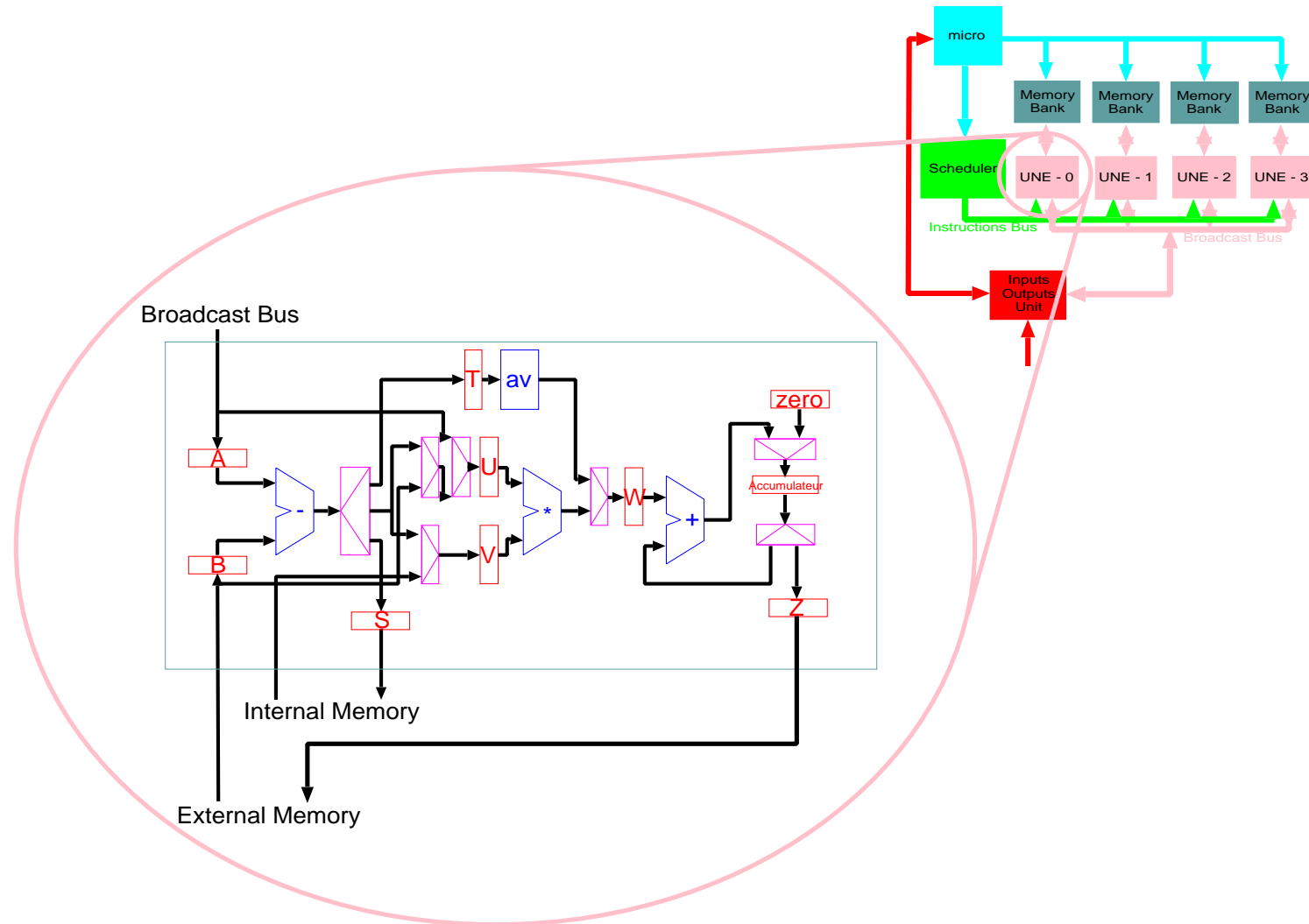
**Memory** Store the parameters of the network

**Input-Output Unit** High Input-Output bandwidth

# MAHARADJA Architecture

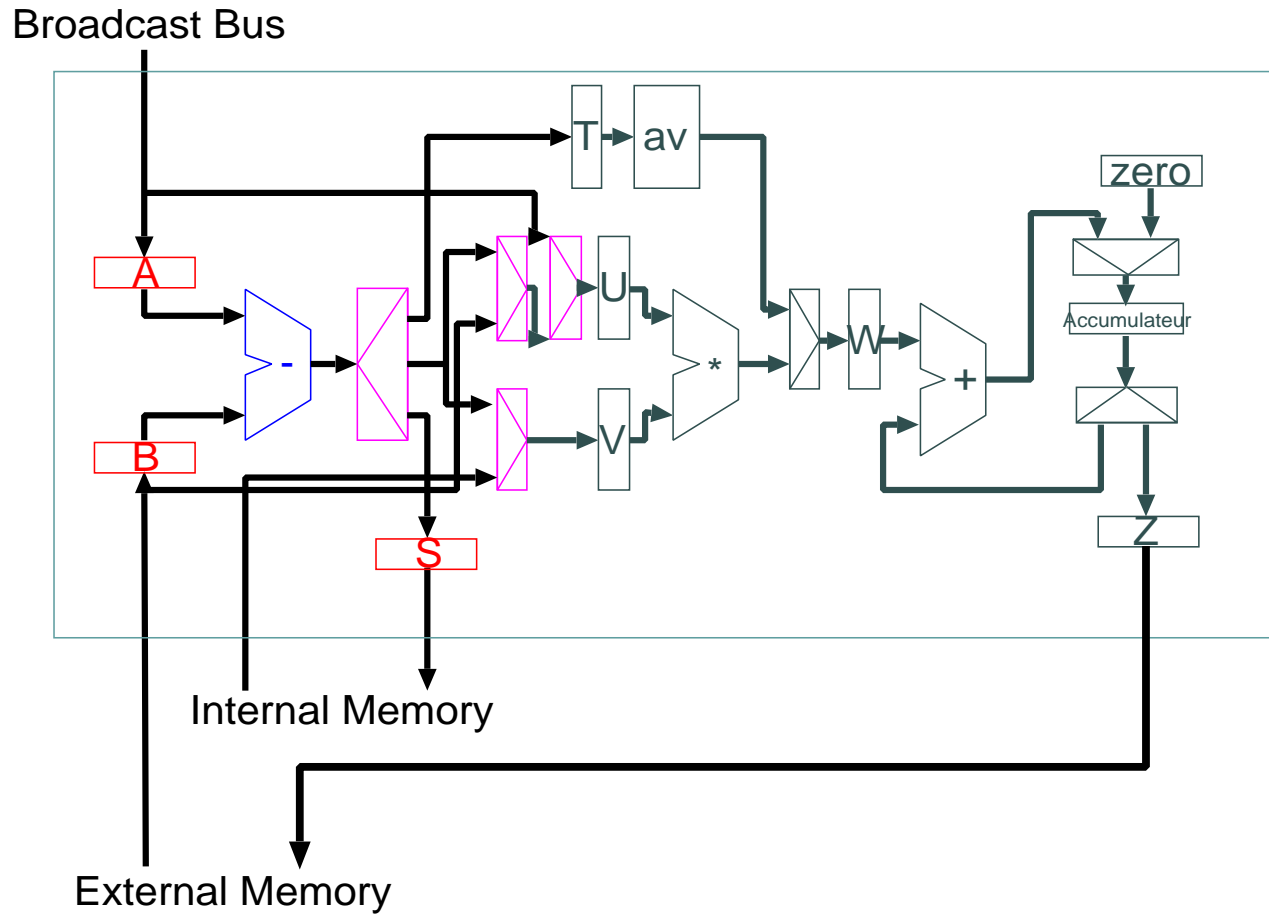


# UNE of MAHARADJA : Internal

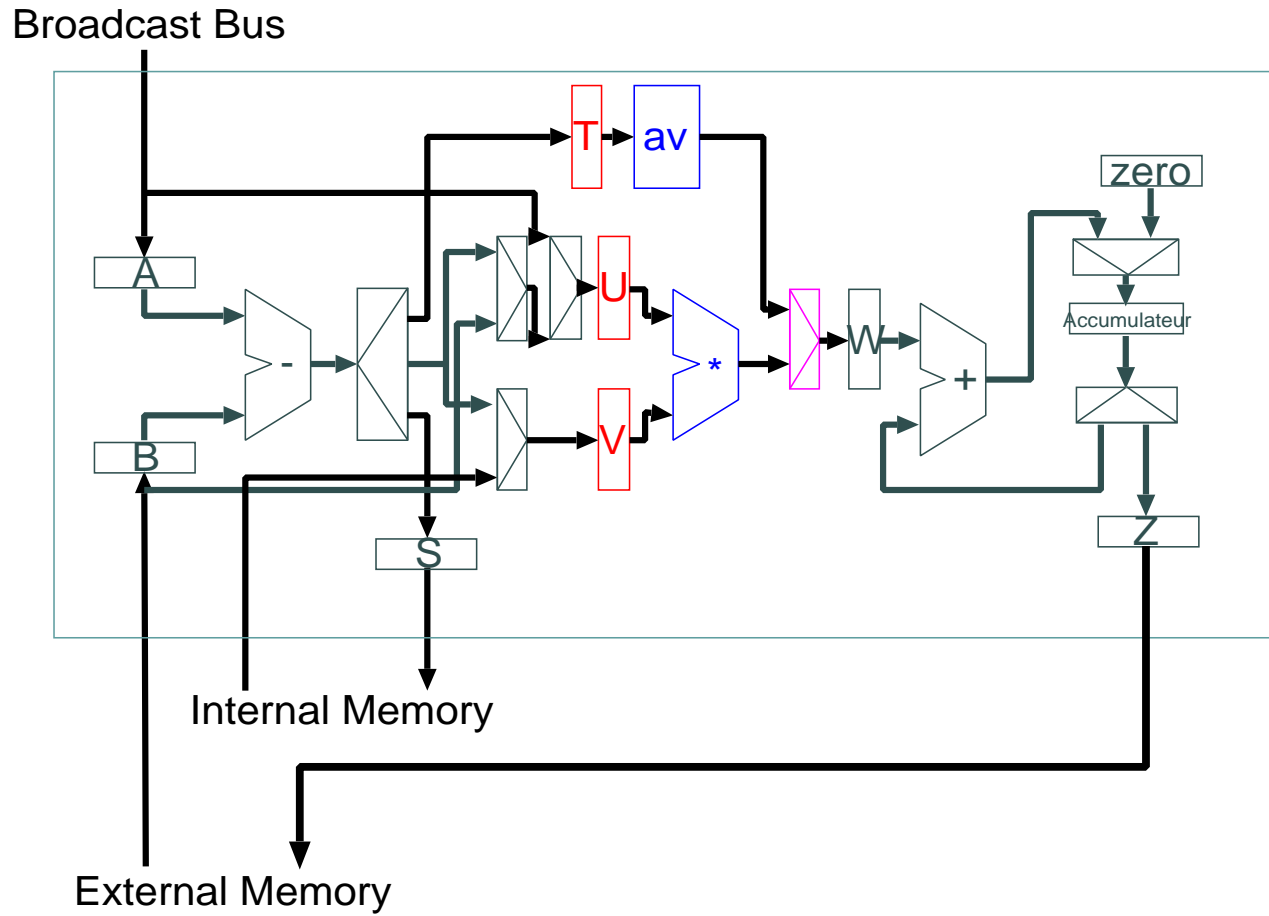




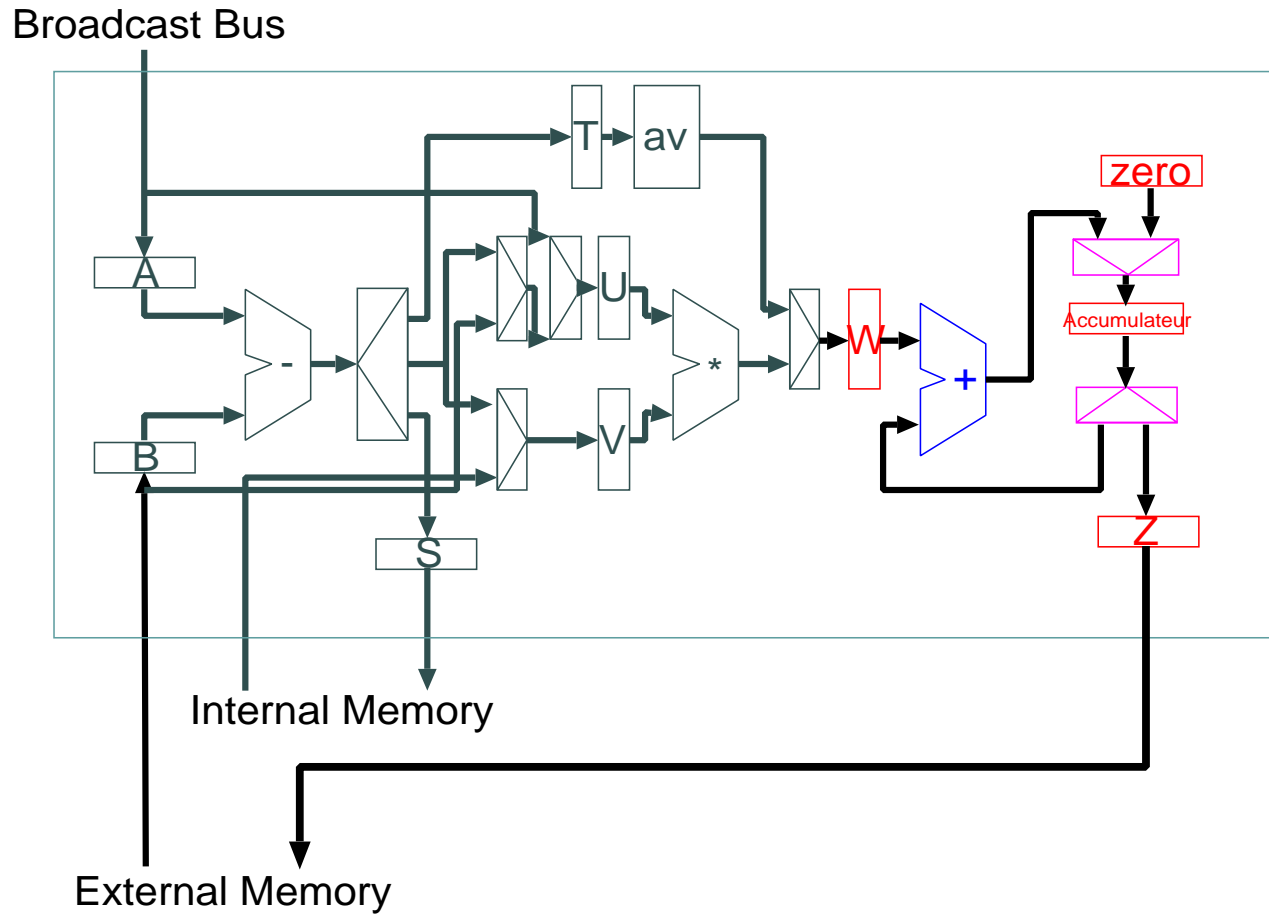
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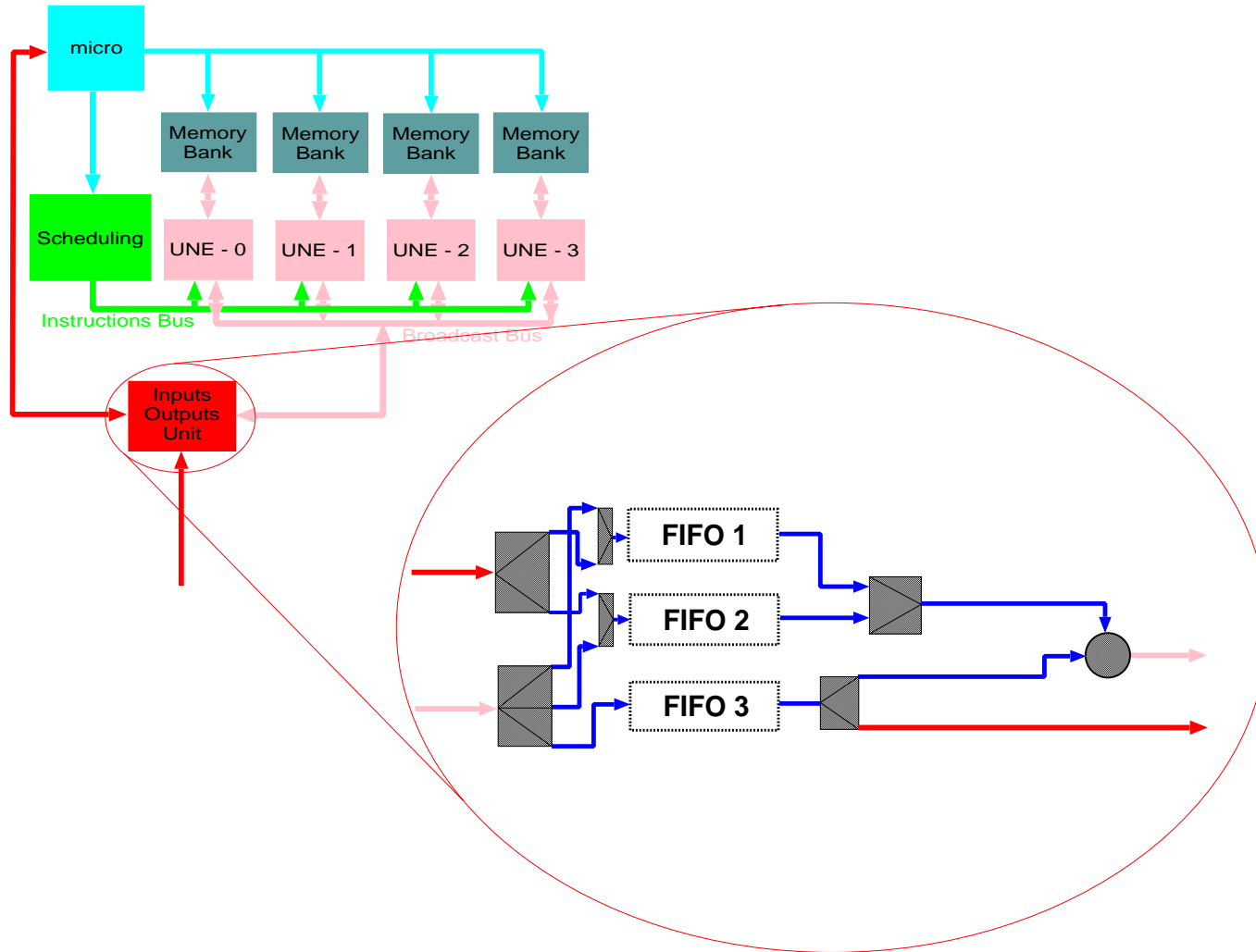
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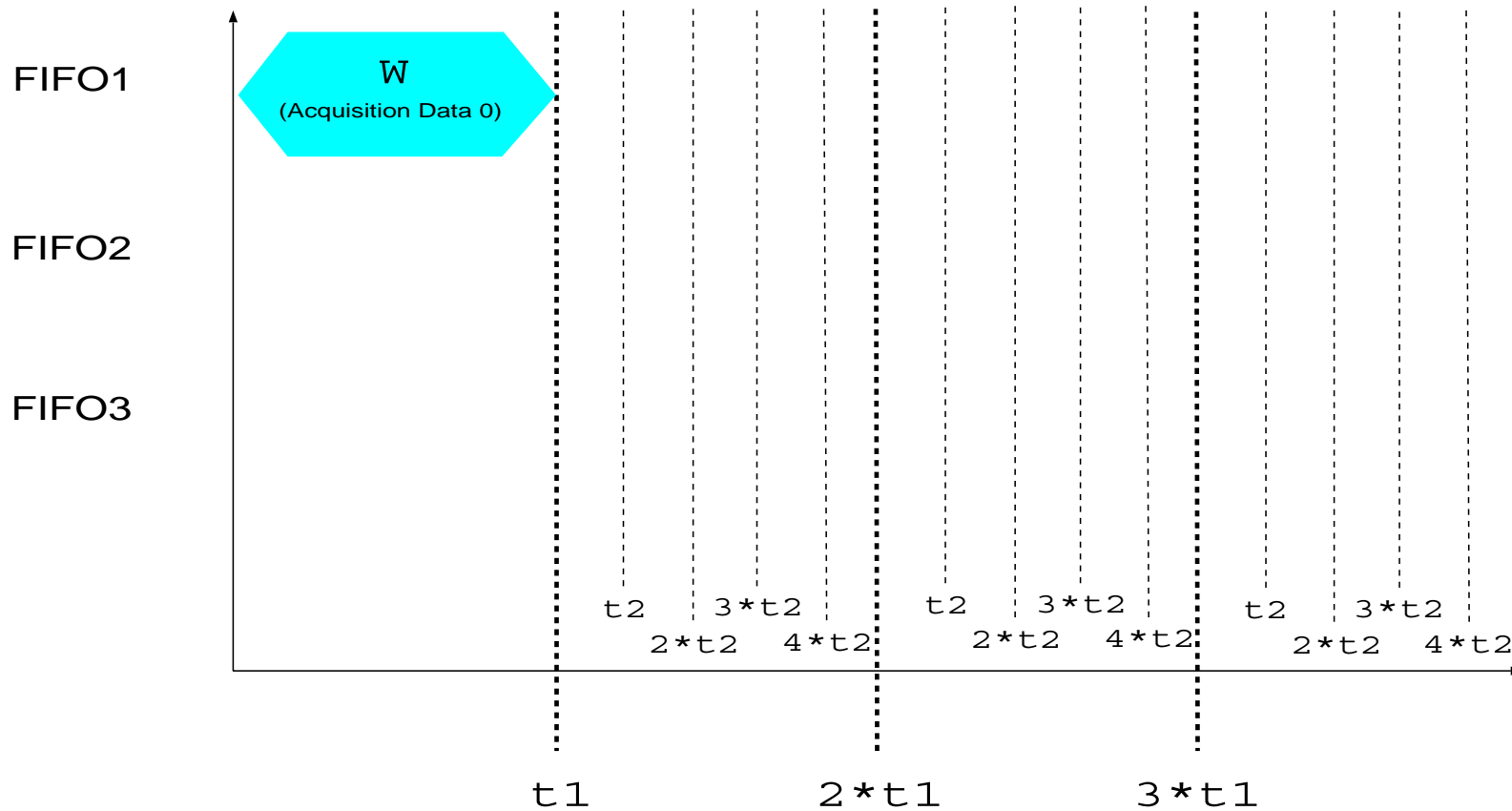
# UNE of MAHARADJA : Internal



# Input-Output Unit of MAHARADJA Architecture



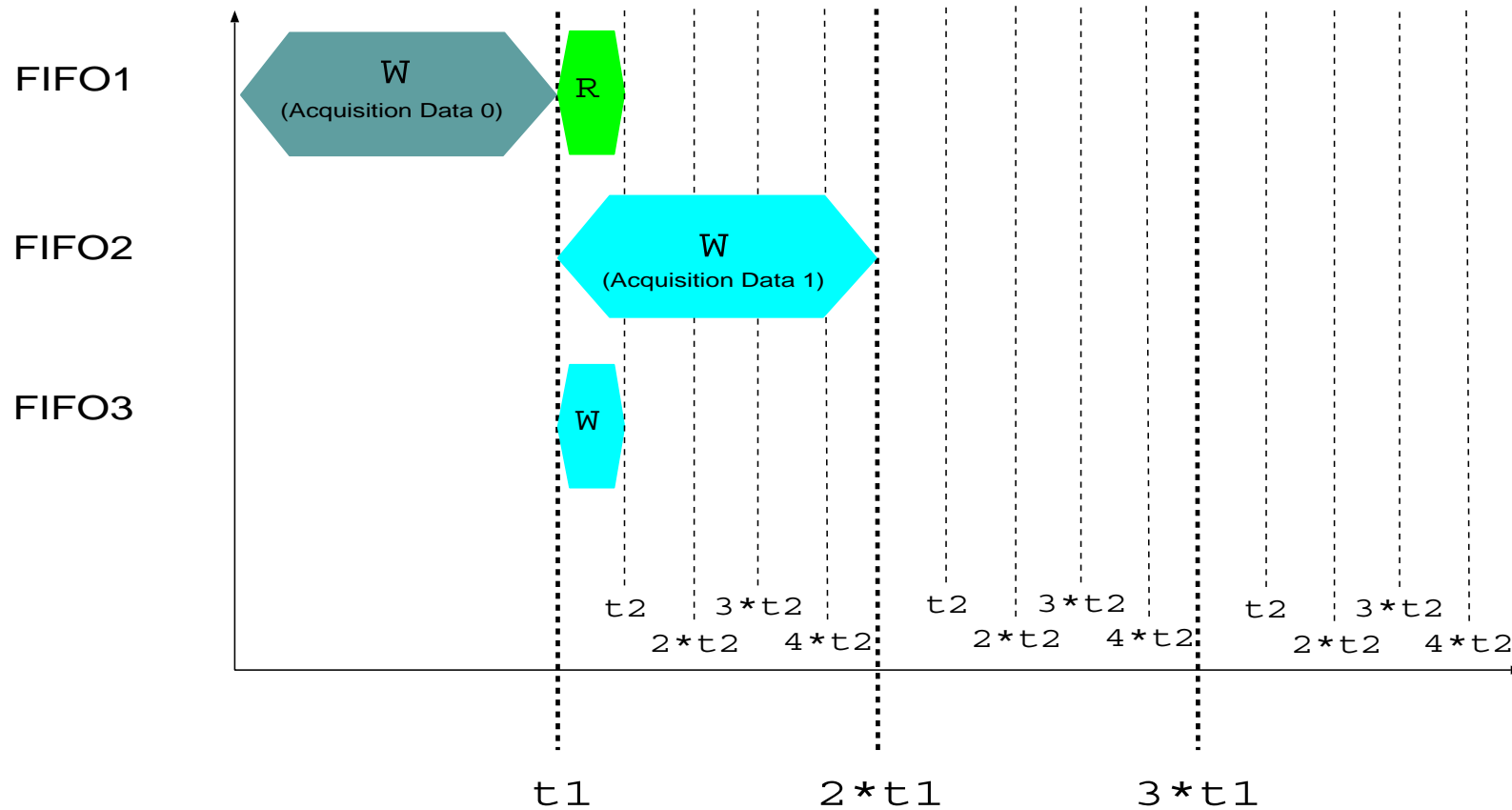
# Principle of Input-Output Unit Ping-Pong scheduling



## Légende :

- $t_1$  : Acquisition period of new data
- $t_2$  : Compute layer period
- R : Fifo reading
- W : Fifo writing

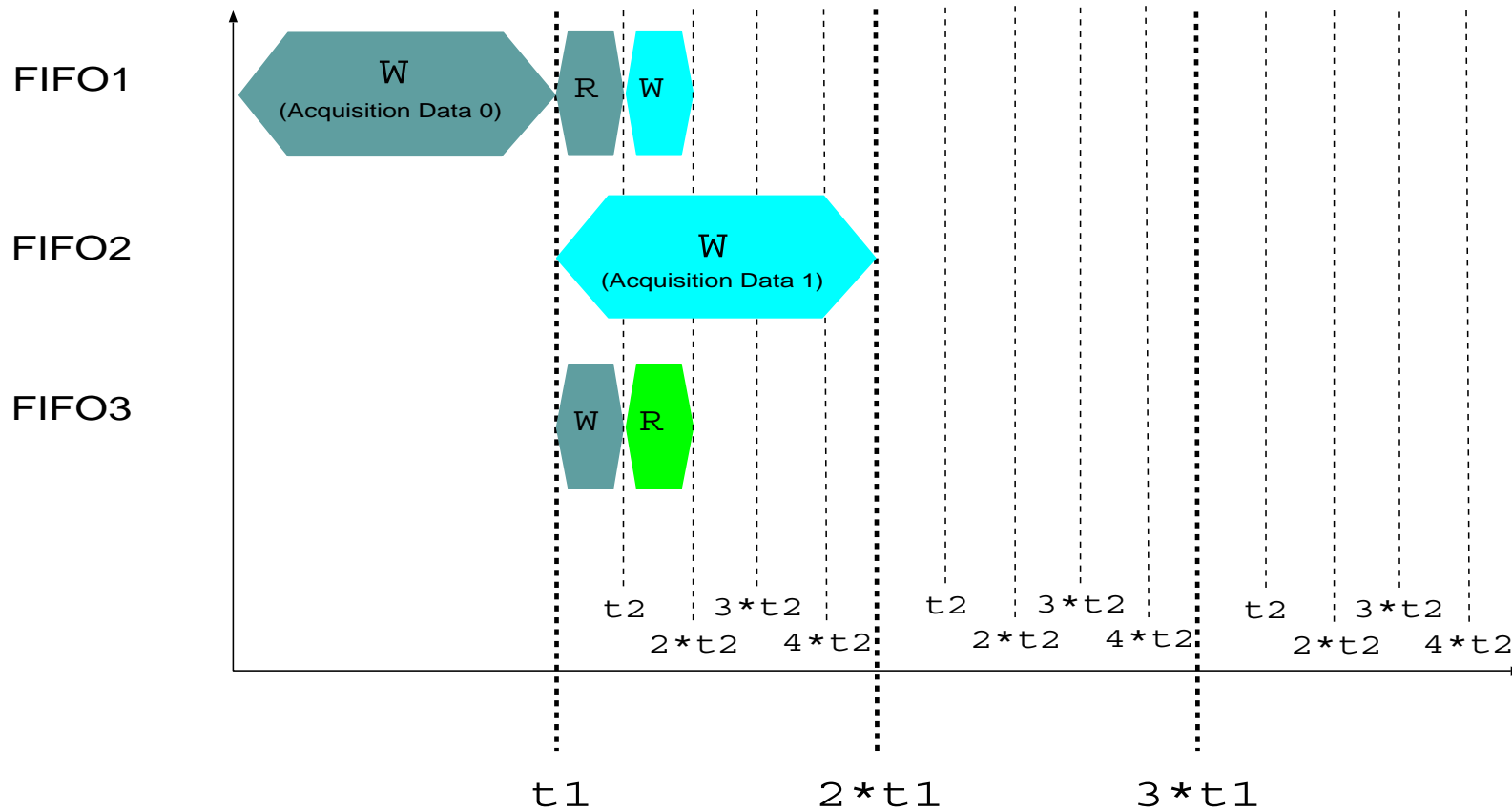
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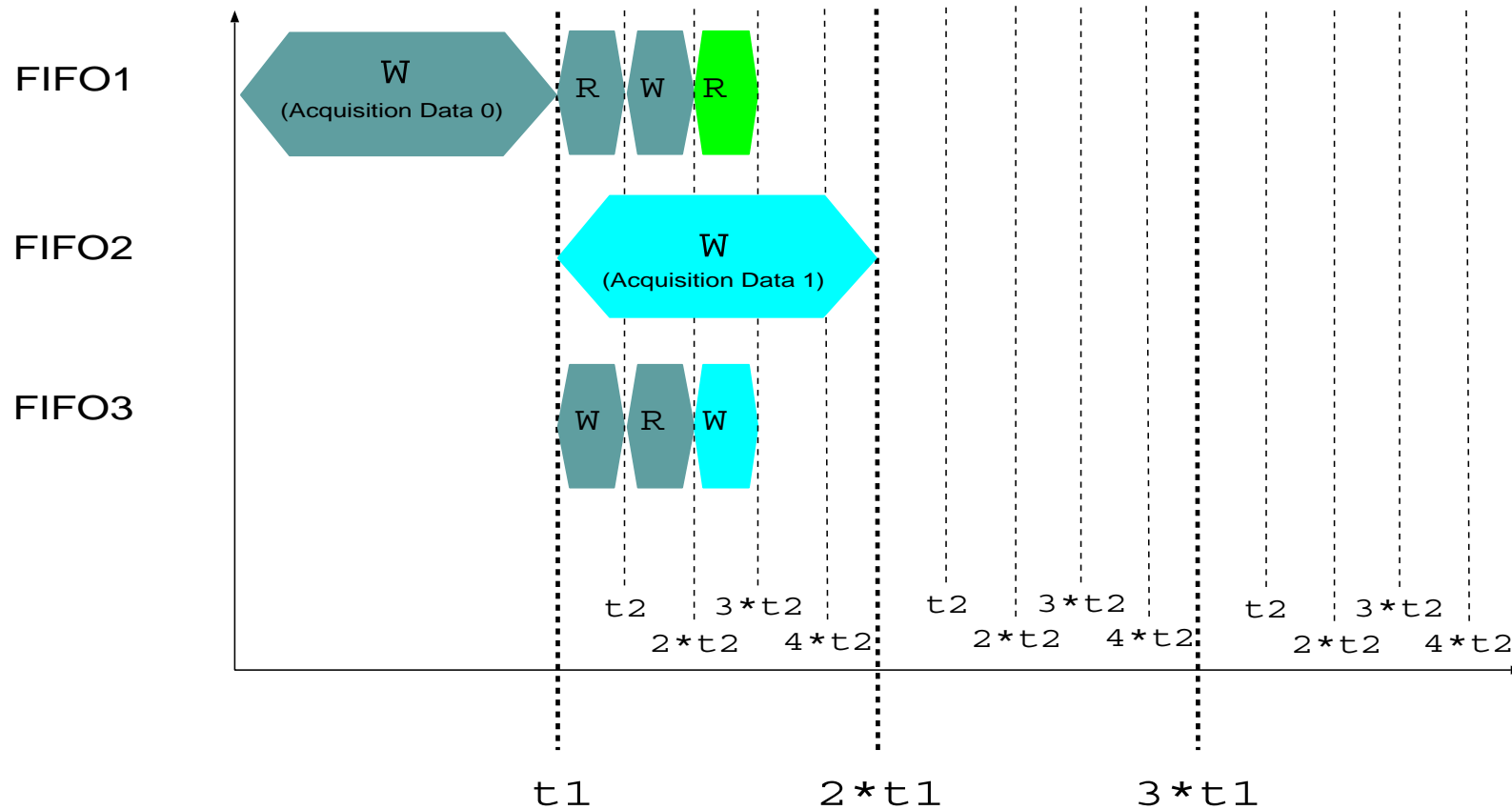
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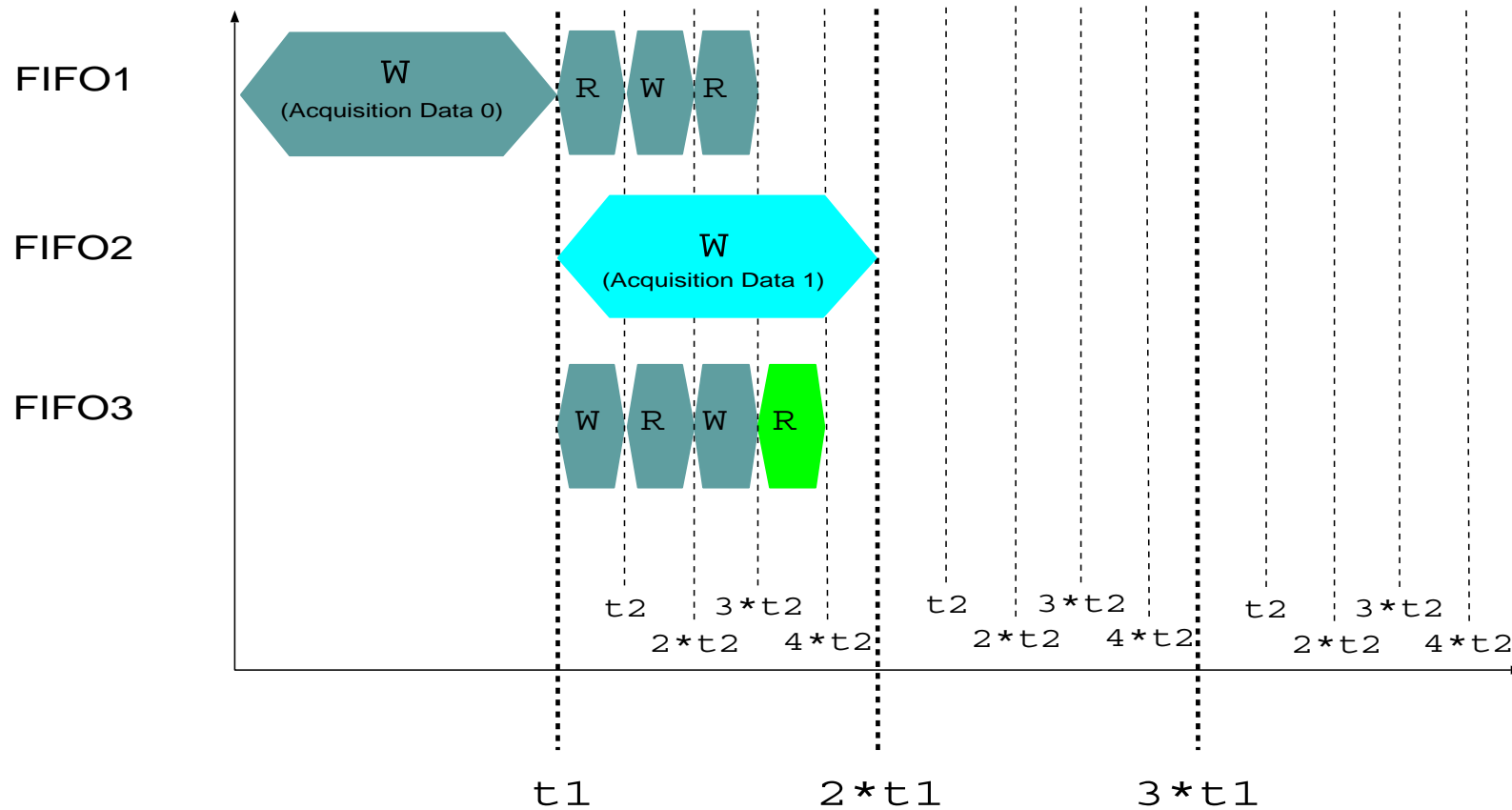


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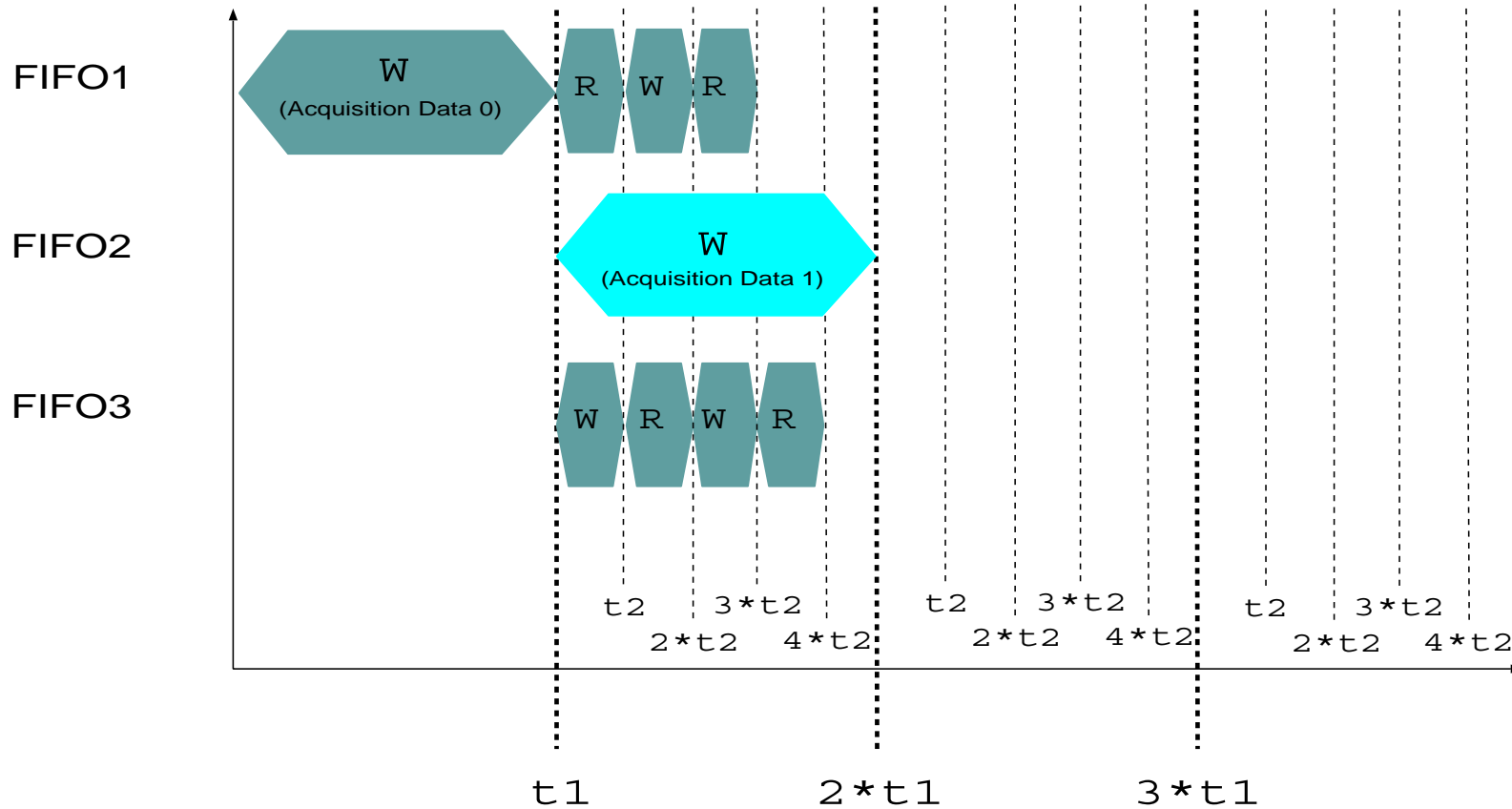
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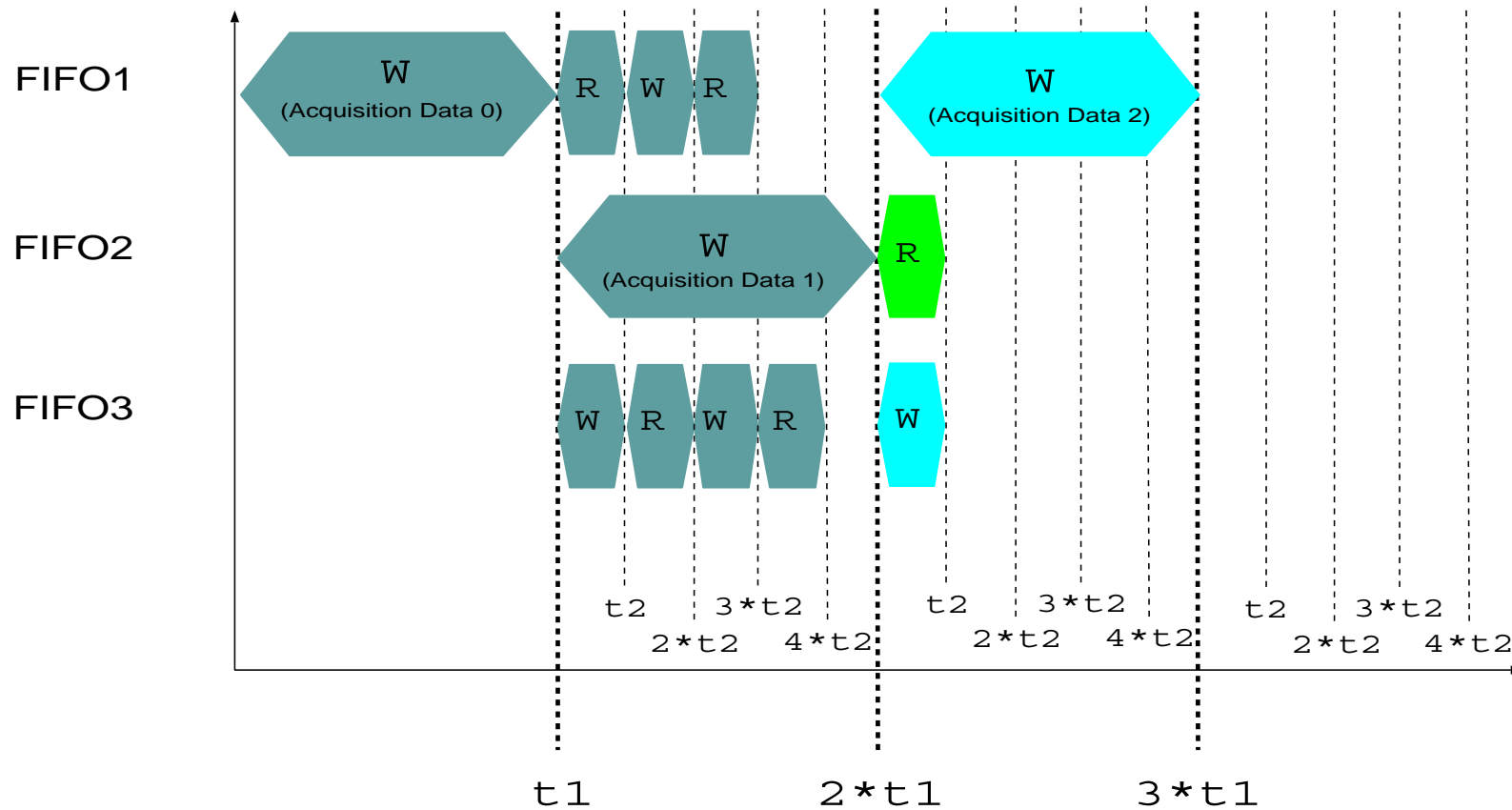
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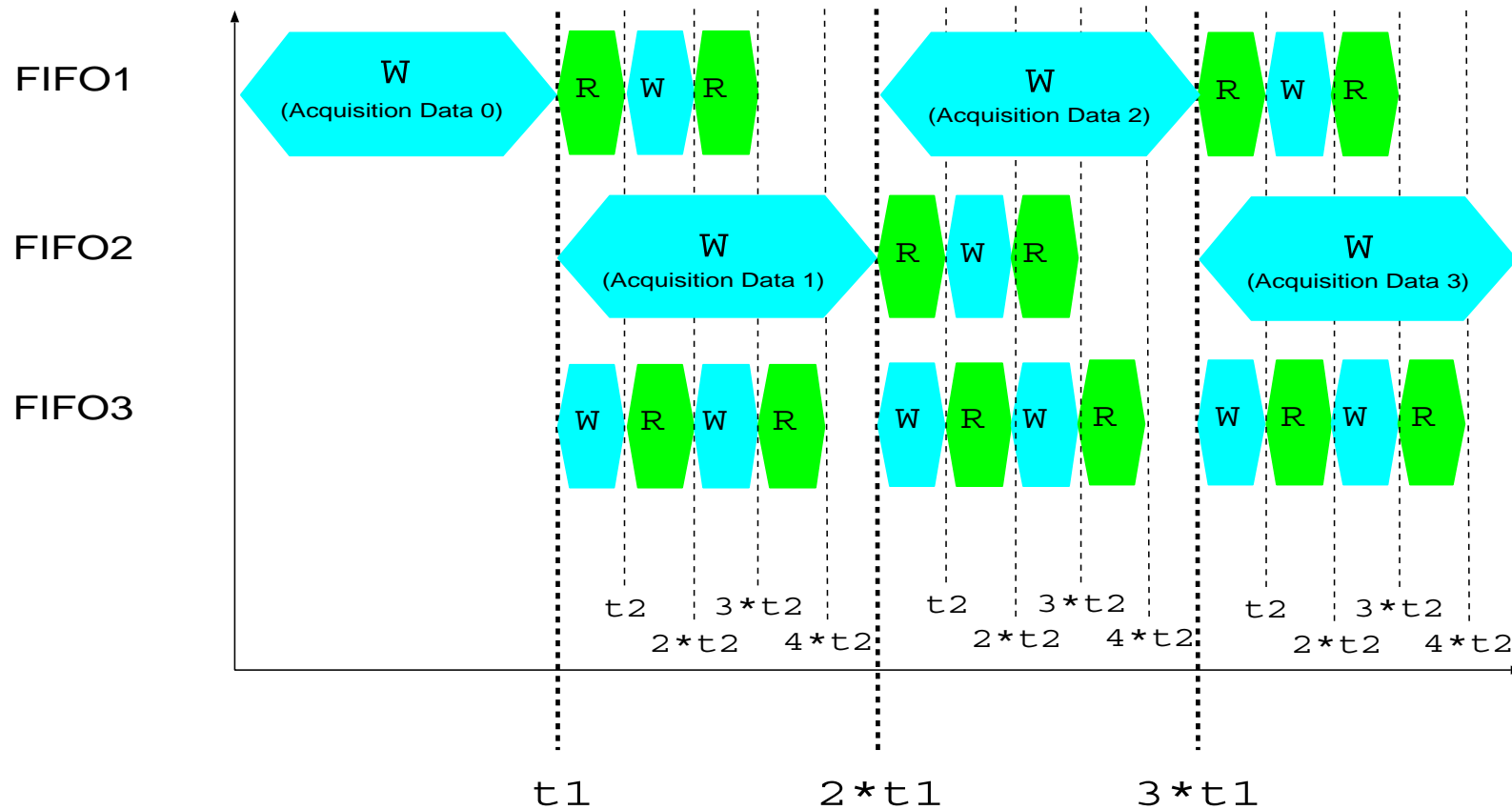
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## What now?

- ☞ Paradigm
- ☞ Prototype is now under development
- ☞ Altera FPGA Apex20k Solution

# Electronic System Methodology Evaluation

- ☞ Neural Networks simulation evaluation performances
- ☞ Time simulation prediction of a neural network
- ☞ Electronic system analysis

## Time analysis of MAHARADJA

$nbp$  : Number of post-synaptic potentials (Terminal layer of the connection)

$nbe$  : Number of neurons (Initial layer of the connection)

### Multi Layer Perceptrons

$$\sum_{i=1}^N \left\lceil \frac{nbe_i}{4} \right\rceil * (nbp_i + 2) + nbe_i + 1$$

### Manhattan Distance

$$\left\lceil \frac{nbp}{4} \right\rceil * (nbe + 4) + \left\lceil \frac{nbe_s}{4} \right\rceil * (nbp_s + 2) + nbe_s + 1$$

### Euclidian Distance

$$\left\lceil \frac{nbp}{4} \right\rceil * (nbe + 4) + \left\lceil \frac{nbe_s}{4} \right\rceil * (nbp_s + 2) + nbe_s + 1$$

### Mahalanobis Distance

$$\left\lceil \frac{nbp}{4} \right\rceil * (nbe^2 + 6 * nbe + 2) + \left\lceil \frac{nbe_s}{4} \right\rceil * (nbp_s + 2) + nbe_s + 1$$

### Time Comparizon

System	Frequence (MHz)	Time ( $\mu$ s)
MAHARADJA 4 UNE	10	6.5
MAHARADJA 8 UNE	10	3.2
MAHARADJA 8 UNE	20	1.6
PENTIUM	800	5
ULTRA SPARC	333	13



## Conclusion

- ☞ MAHARADJA simulate the MLP neural networks
- ☞ Real time simulation of RBF and MLP
- ☞ Satisfy  $\mu s$  time constraint.