Silicon Tracking Detectors

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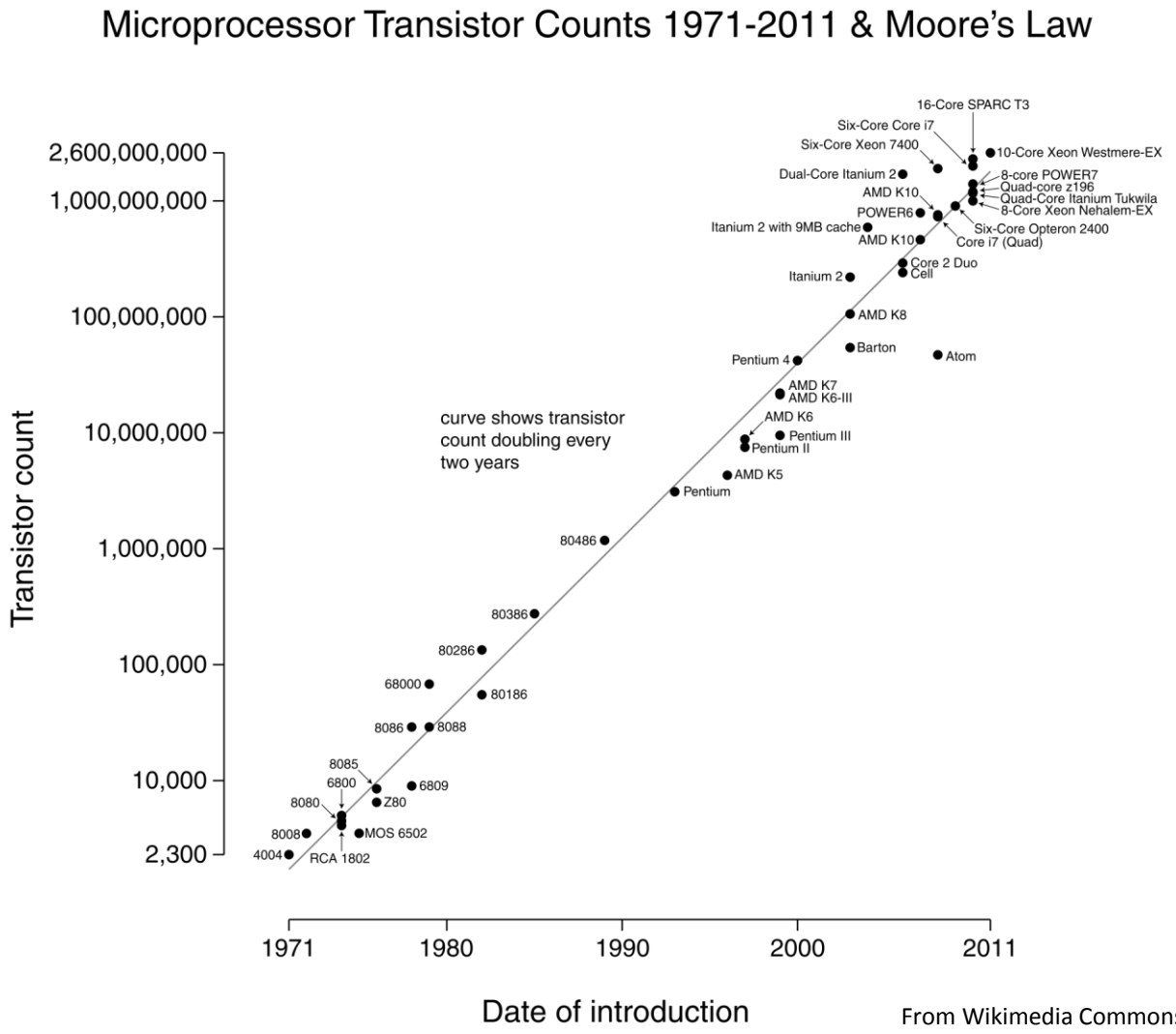
Fermilab

Outline

- Introduction – Why Silicon?
  - Material properties + IC technology
- Basics
  - Diode junction
  - Depletion voltage
- History
- Radiation Damage
- Variety of Sensor Types

Leverages IC Technology



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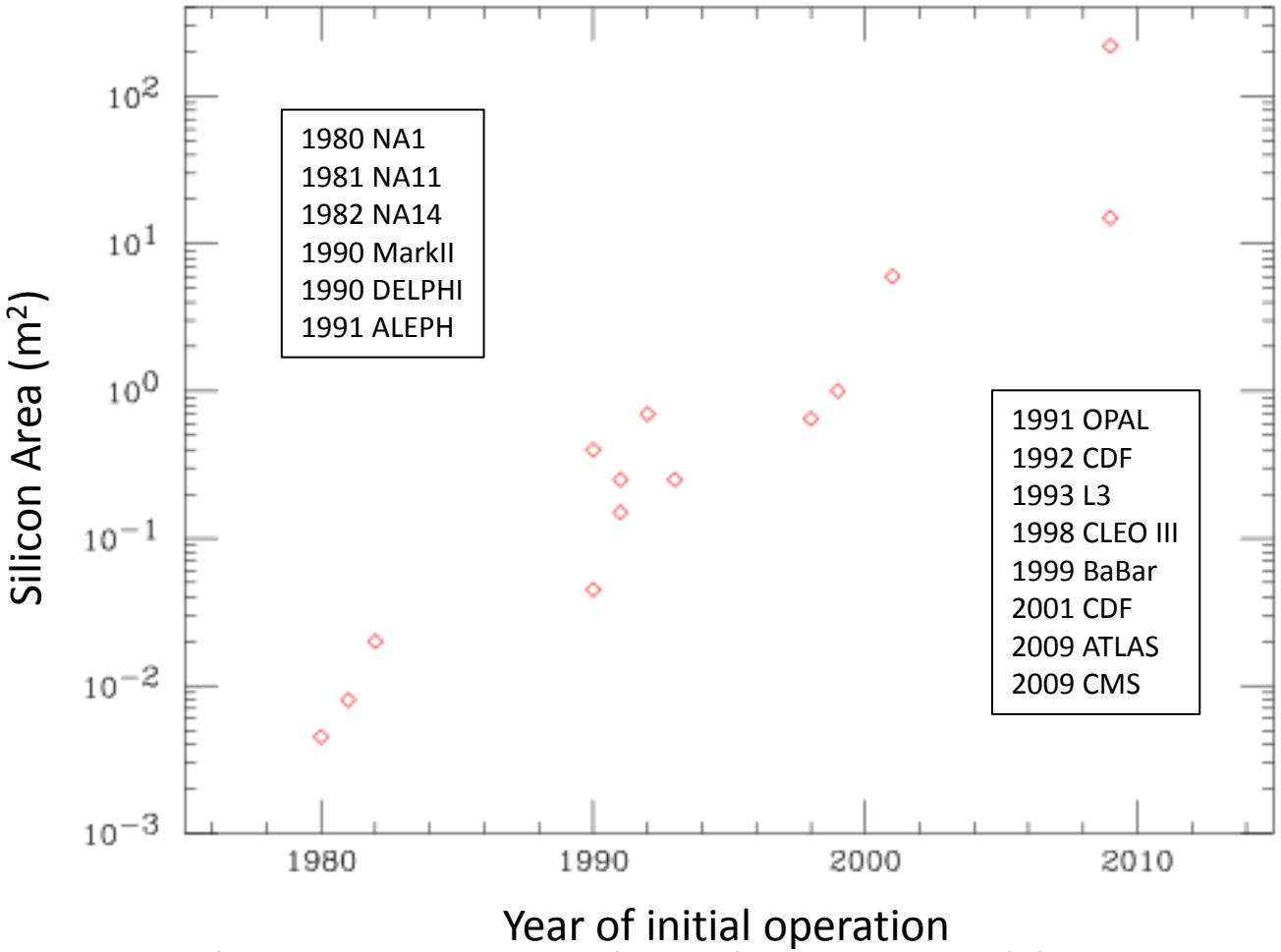
Exponential improvements of silicon ICs WILL end someday… but when?

Silicon Detectors in HEP (representative selection, appox dates)



Silicon detectors also continue to be improved in surprising ways – size is only one.

Stolen from someone (can't remember who)

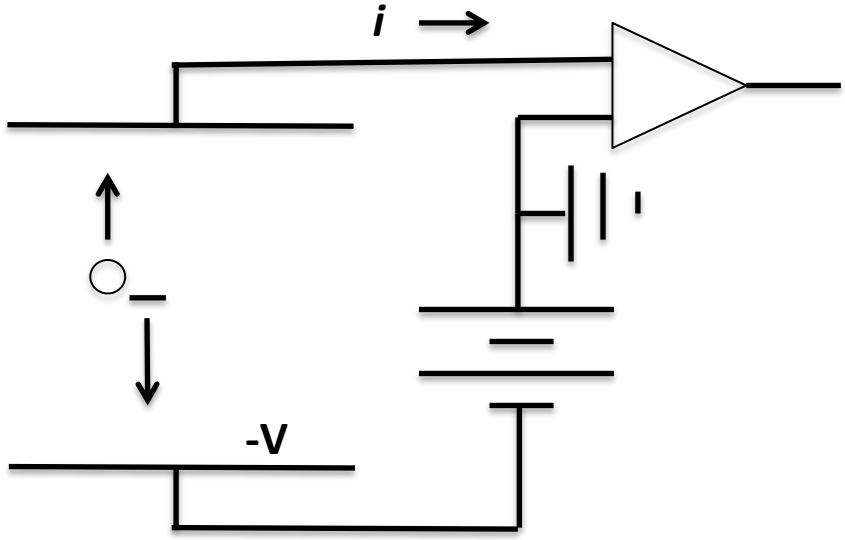
Why Silicon Detectors?
Material Properties enable Excellent Energy Resolution

- Any energy deposition with E>band gap can create a detectable e-h pair → large number of charge carriers
- Long charge carrier lifetime in (achievable) crystals
- Large number of charge carriers → small statistical fluctuation of the number → good energy resolution

Material	Average energy to create 1 mobile charge carrier (pair)
NaI (gold standard)	>50 eV (per scin. γ – doesn't include detection QE)
Si	3.62 eV (band gap = 1.12 eV)
Ge	2.98 eV (band gap = 0.74 eV)
CdTe	4.43 eV (band gap = 1.47 eV)
Ar	26 eV
Xe	22 eV

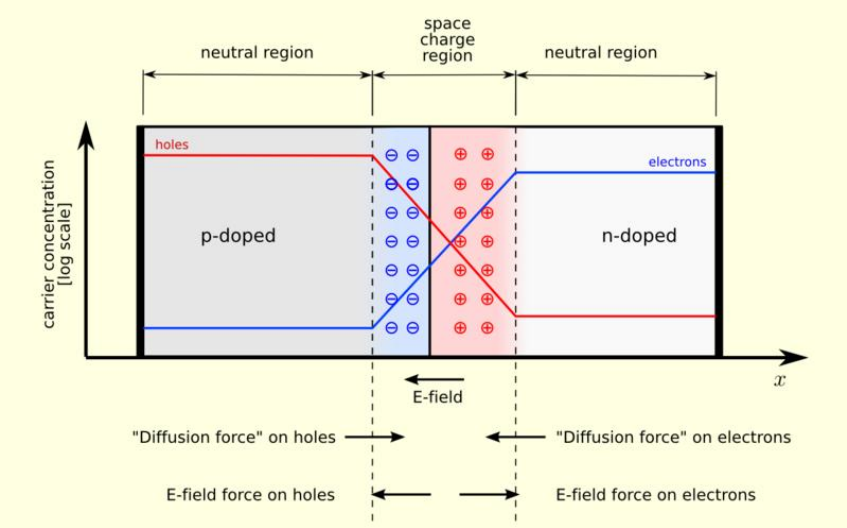
Silicon Detector Basics

- Most silicon detectors are ionization detectors (no gain)
- Ionizing radiation creates electron/hole pairs
- Charge carriers move in applied E field
- Motion induces a current in an external circuit, which can be amplified and sensed.
- ***However, free carriers must first be removed so the applied voltage doesn't simply result in a (large) DC current – this is usually accomplished with a reverse biased diode.***

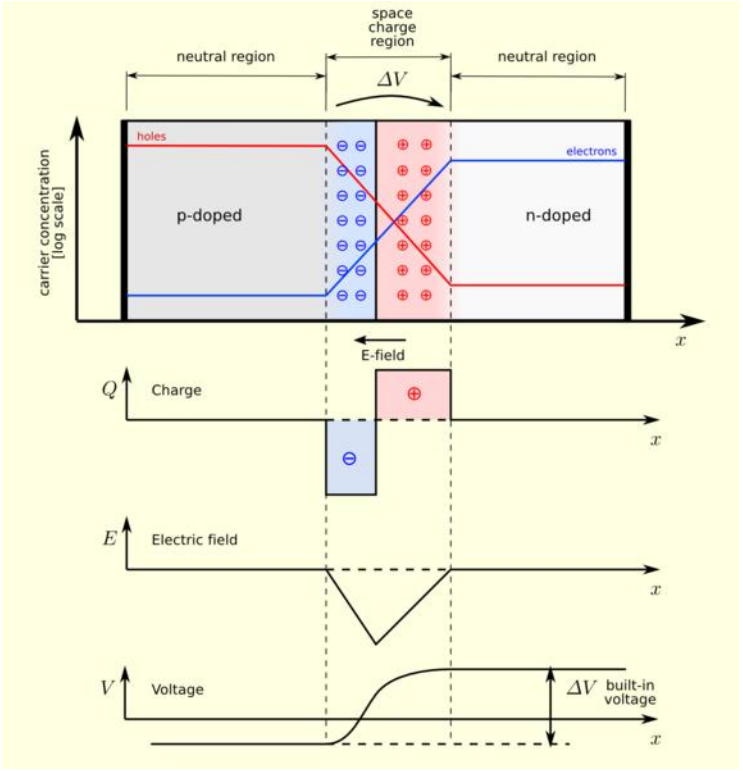


pn Diode Junction

Free charges move until the chemical potential is balanced by an electrical potential



The space charge region is also called the depletion region because it has been depleted of free charges.



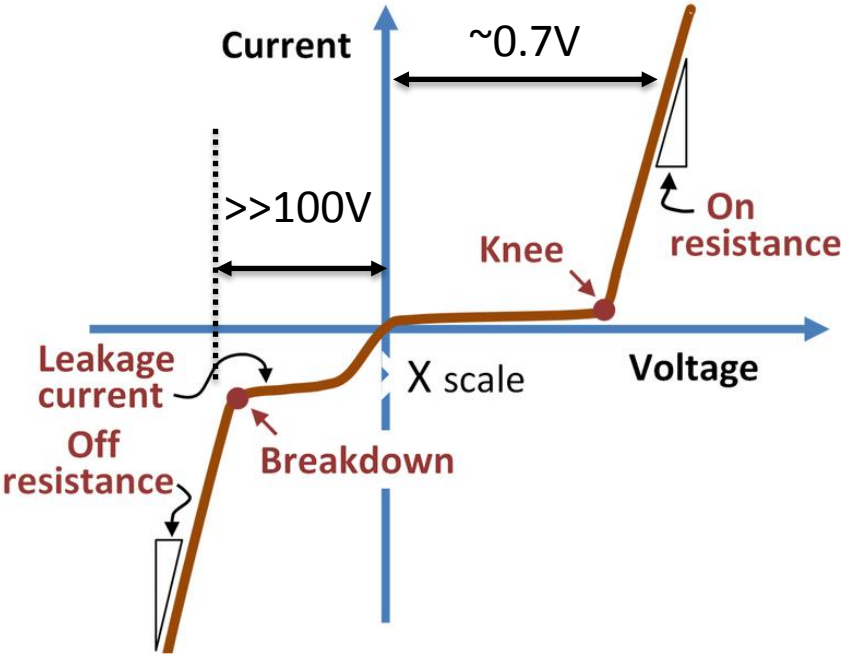
PIN Detectors

- If the p and n layers are created on either side of a nearly pure silicon crystal, the result is a PIN structure (I = intrinsic).
- In this case, the depletion layer is thicker than in a pn junction.
- Ionizing radiation can create additional free charges, which move in the field created by the junction & can induce a signal in an external circuit.
- Example = sensor for garage door opener

- In practice, the nearly pure layer is either lightly doped n-type or lightly doped p-type material
- If n-type, there is a pn junction on the p side & an n-/n+ ohmic contact on the n side.
- If p-type, there is a p+/p- ohmic contact on the p side and an np junction of the n side.
- Lightly doped region can be depleted of free charge by reverse biasing the diode junction.

Diode Characteristic

- Applied voltage in the same direction as the built-in voltage results in large current
- Voltage applied in the opposite direction (reverse bias) results in almost no current; it simply draws more free charge from the bulk into the junction, increasing the size of the depletion region.



Depletion Voltage

- Reverse bias draws free charges into the diode junction from nearby bulk silicon, leaving the bulk electrically charged & reducing the electric field (due to the applied bias voltage) at points away from the junction
- The "depletion depth" is the distance at which the field due to the uniform space charge in the depleted region exactly balances the applied voltage and is easily calculated:

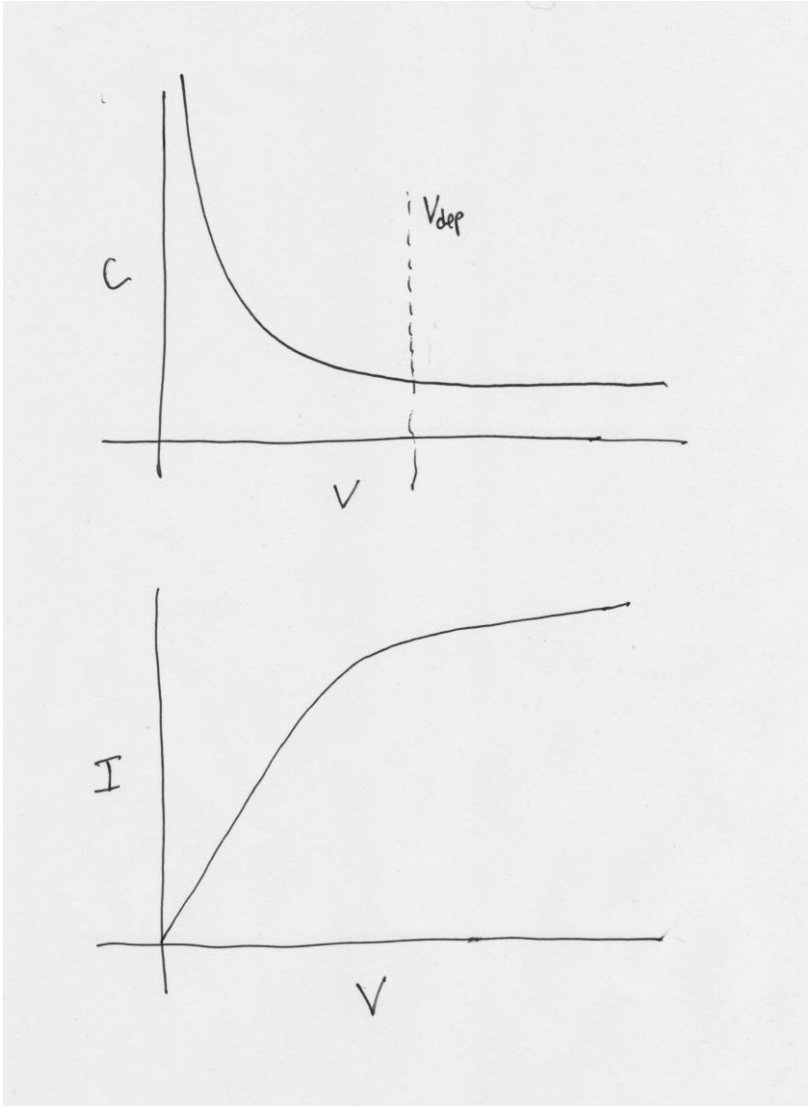
$$V = \frac{qd^2N}{2\varepsilon} \text{ or } d = \sqrt{\frac{2\varepsilon V}{qN}}$$

(ε = permittivity of silicon; N = # of free charges = # of dopant sites in volume)

- The "depletion voltage" is the voltage required to remove all free charges from the bulk; this occurs when *d* = the thickness of the sensor.

Measuring Depletion Voltage

- A silicon detector has a (junction) capacitance that is given by geometry:
  $C = \frac{A\varepsilon\varepsilon_0}{D}$
  - ε = silicon dielectric constant
  - ε_0 = permittivity of free space
  - A = junction area
  - **D = Depletion Depth**
- V_{dep} is best measured by CV curve.
- Can also be determined (less well) from IV



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- Introduction – Why Silicon?
- Basics
  - Diode junction
  - Depletion voltage
- **History**
- Radiation Damage
- Variety of Sensor Types

First Development – Nuclear Physics (γ-ray spectroscopy)

- 1959: Gold surface barrier (Si) diode: J.M. McKenzie and D.A. Bromley, Bull. Am. Phys. Soc. 4 (1959) 422.
- 1960's: Development of lithium "drifted" thick detectors: J.H. Elliott, NIM 12 (1961) 60.
  - Start with p-bulk, use lithium to create an n-p junction on one surface, reverse bias the junction at ~150C (in an oven) – lithium diffuses into the bulk making it nearly intrinsic allowing depletion of thick device without breakdown.

Position Resolution

- High stopping power of silicon → almost all free charge is created within a few microns of the path of a charged particle.
- **Silicon IC technology (planar processing) is key**
  - Photolithography to create micron-scale features (strip diodes)
  - Doping by diffusion and ion implantation
  - SiO_2 passivation
    - Cut edges are conductive; surface would be too without passivation
  - J. Kemmer, NIM 169 (1980) 449 and NIM 226 (1984) 89

First use in HEP – Charm Experiments

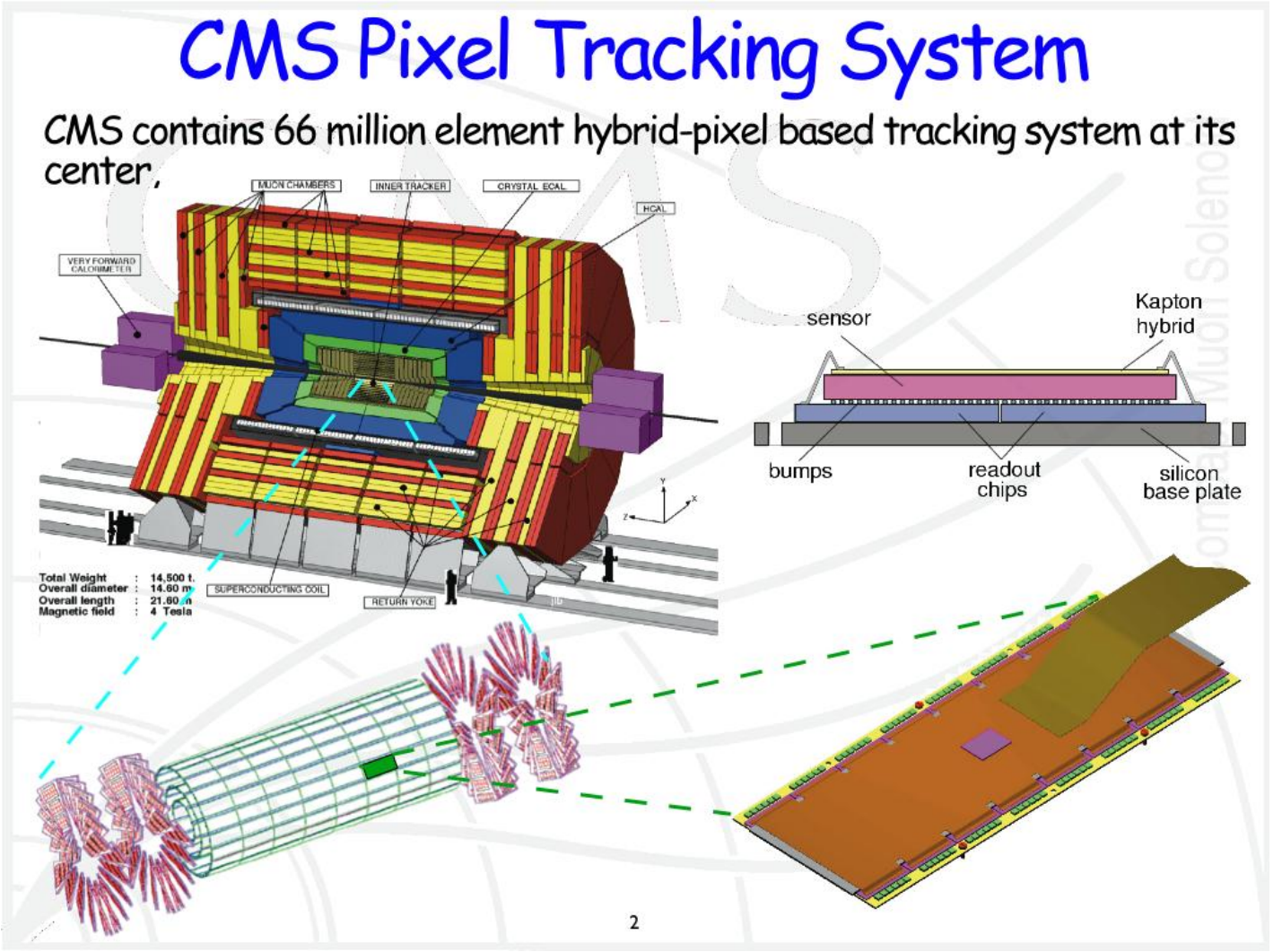
- 1981 – 1985:
  - CERN NA11 (First planar devices): Home built & with Enertec/Schlumberger… later Eurisys Mesures, now Canberra Eurisys.
  - CERN NA14: Development with Centronic starting in 1981; in 1983 Wilburn & Lucas formed Micron & development continued.
  - Fermilab E653: Established R&D relationship with Hamamatsu in 1981 and contracted with Micron in 1983 (Hamamatsu SSDs with 12.5μ pitch used in 1987).

Breakthrough

- Fermilab E691 (Tagged Photon Experiment):
  - Used NA14-type sensors from Micron.
  - Coupled to working spectrometer, and a high flux tagged photon beam with good duty factor made possible by 800 GeV Tevatron
  - Inclusive trigger (almost min bias) & high rate DAQ
  - First use of massively parallel computer “farm”

- Yielded definitive measurements of charm particle lifetimes and **established silicon detectors as an essential component of the detector builder’s “kit.”**

The State of the Art



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Radiation Damage – An R&D tale

- Basics have “always” been well known
- Nuclear interactions displace silicon atoms from their lattice position, creating interstitials & vacancies and corresponding energy states in the band gap.
- Leakage current increases
- Bulk material acts more “p type” as more defects act as acceptors than as donors
- Damage is partially reversible (temperature dependant annealing occurs)
- “Reverse annealing” also occurs; presumably associated with the formation of divacancies, or other defect complexes with unfortunate energy levels.

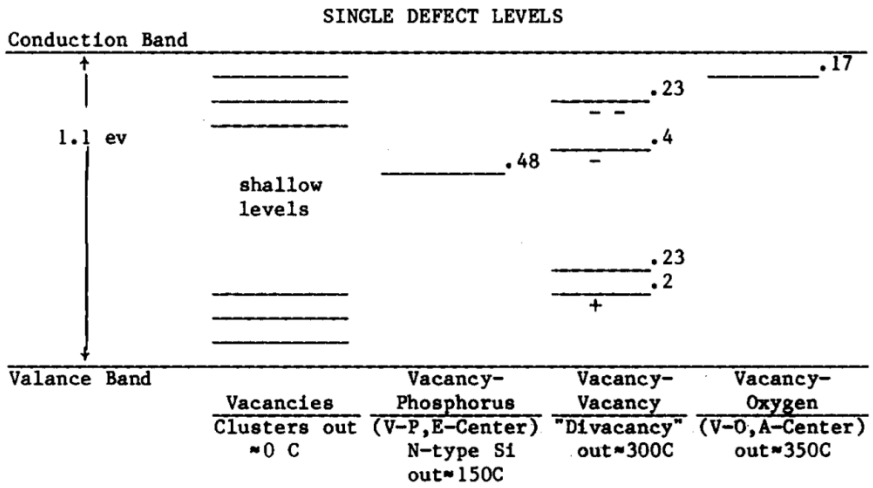


Fig. 1. Level diagram.

From Kraner, NIM 225 (1984) 615-618

Quantifying Flux for (Bulk) Radiation Damage Studies

- The conjecture that bulk damage is proportional to the total KE imparted to displaced silicon atoms is called “the NIEL hypothesis.” NIEL = Non Ionizing Energy Loss.
- Charged hadrons lose energy in silicon primarily by multiple Coulomb scattering, which does not displace silicon atoms (only a small fraction of the energy loss is caused by strong interactions with silicon nucleii)
- Bulk damage is expressed in terms of the damage that would be caused by a given flux of neutrons… but this depends on the neutron energy.
- It is conventional to use 1 MeV neutrons as the benchmark (American Society for Testing and Materials E772-94)

NIEL, KERMA, & all that

- KERMA = Kinetic Energy Released in MAtter

$$KERMA(keV) = NIEL(keV\,\frac{cm^2}{gm}) \times \phi(\frac{\#}{cm^2}) \times wt(gm)$$

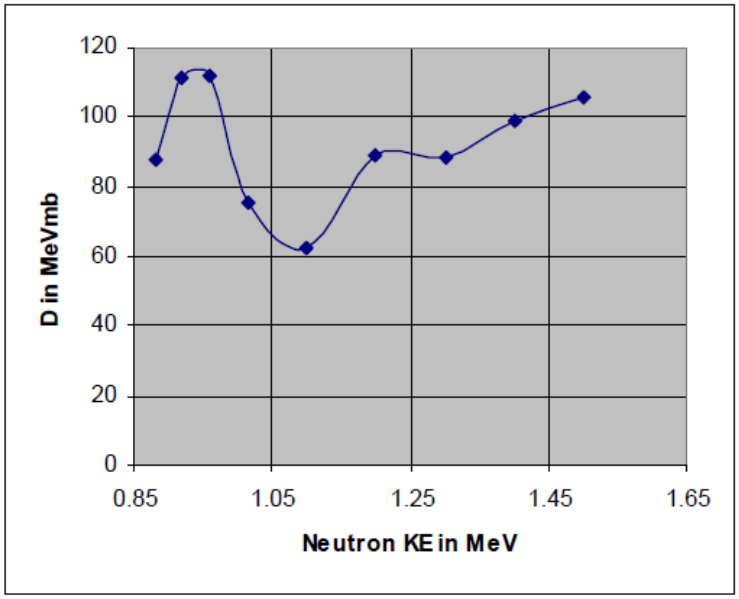
- Often given in terms of the "displacement damage cross section" D

$$KERMA(MeV) = D(MeVmb) \times \phi(\frac{\#}{cm^2}) \times (\#Si) \times (\frac{10^{-27}\,\mathrm{cm}^2}{\mathrm{mb}})$$

- To confuse things, D is often called NIEL

Definition of 1 MeV n-equivalent

- Unfortunately, the displacement damaged caused by ~1 MeV neutrons is a strong function of energy. As a result, the ASTM standard specifies that a "[1 MeV]neutron displacement kerma factor" of 95 MeVmb shall be used when calculating the equivalent 1 MeV neutron fluence for an irradiation.



Neutron displacement damage as a function of energy, from E 722-94 (1998 Annual Book of ASTM Standards)

Leakage Current

- Leakage current is proportional to flux and depends exponentially on temperature. It scales with NIEL.
- Assuming effective guard rings, leakage current is entirely bulk generated. The current is reduced by beneficial annealing. It is proportional to silicon volume and to effective flux. This dependence is reflected in the following formula by making α a function of both time and temperature: $I = \alpha \Phi_{eq} V$
  - Immediately after irradiation, α(room temp) $\approx$ 6E-17 A/cm. This drops to about 2E-17 after a long time.
  - The official ROSE value of α is measured at room temperature, after 80 minutes annealing at 60 °C, and is 4E-17 A/cm.
  - Leakage current is proportional to $T^2 \exp(-E_g/2kT)$ (Eg = band gap energy = 1.12 eV; k = Boltzman constant = 8.62E-5 eV/degree K).
  - Leakage current can be a problem for Strip detectors for two reasons:
    - **It can saturate a charge integrating amplifier**
    - **It can lead to thermal runaway**

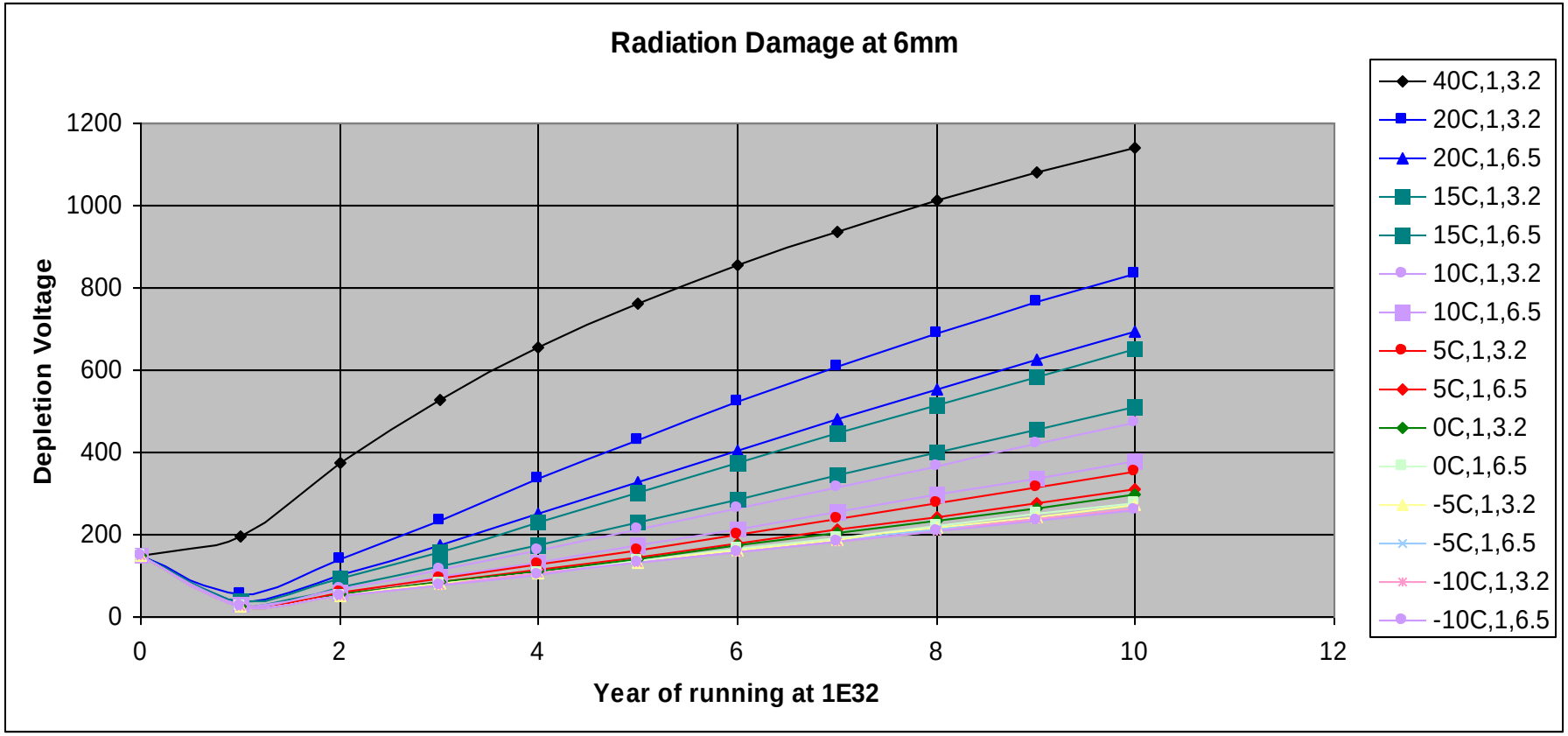
The Hamburg Model

- Parameterization developed by Michael Moll (Ph.D. dissertation) & CERN RD48 (ROSE): damage expressed in terms of a change in the "effective" doping (becomes more p type) $N_{eff} = N_0 + \Delta N_{eff}$
- $\Delta N_{eff}(\Phi_{eq},t(T_a)) = N_A(\Phi_{eq},t(T_a)) + N_C(\Phi_{eq}) + N_Y(\Phi_{eq},t(T_a))$
  - T_a = Annealing temperature.
  - 1st term represents beneficial annealing: $N_A(\Phi_{eq},0) = N_A(\Phi_{eq})$; $N_A(\Phi_{eq},\infty) = 0$.
  - 2nd term represents stable damage & has 2 components, donor removal and acceptor generation. For large doses, acceptor generation is dominant.
  - 3rd term represents reverse annealing: $N_Y(\Phi_{eq},0) = 0$; $N_Y(\Phi_{eq},\infty) = N_Y(\Phi_{eq})$
- Beneficial annealing time constant is ~ 2-3 days at 23°C.
- Reverse annealing time constant is ~ 1.3 yr at 23°C for standard silicon, & 3 – 6.5 yrs at 23°C for oxygenated silicon.
  - Reverse annealing deviates from exponential for long times.
  - Reverse annealing of damage due to charged hadrons (*not* neutrons) saturates for oxygenated silicon (*not* for normal silicon).
- For oxygenated sensors, damage does not scale with NIEL. Damage by neutrons is ~the same as for non-oxygenated sensors, but damage by charged hadrons is reduced. This is true at least for the 2nd & 3rd terms above.

The Hamburg Model - Conclusions

- Both beneficial and reverse annealing are “frozen out” at –5 °C.
- Optimal scenario: run cold; heat up for ~2 weeks/yr.
  - Reduces leakage current
  - Allows beneficial annealing, but ~no reverse annealing.
  - Only the stable damage term remains.
- CDF and D0 ran cold, tried to stay cold always.
- ATLAS & CMS run cold, warm up periodically to allow beneficial annealing.

Example (computed for BTeV pixel detector in 2002)

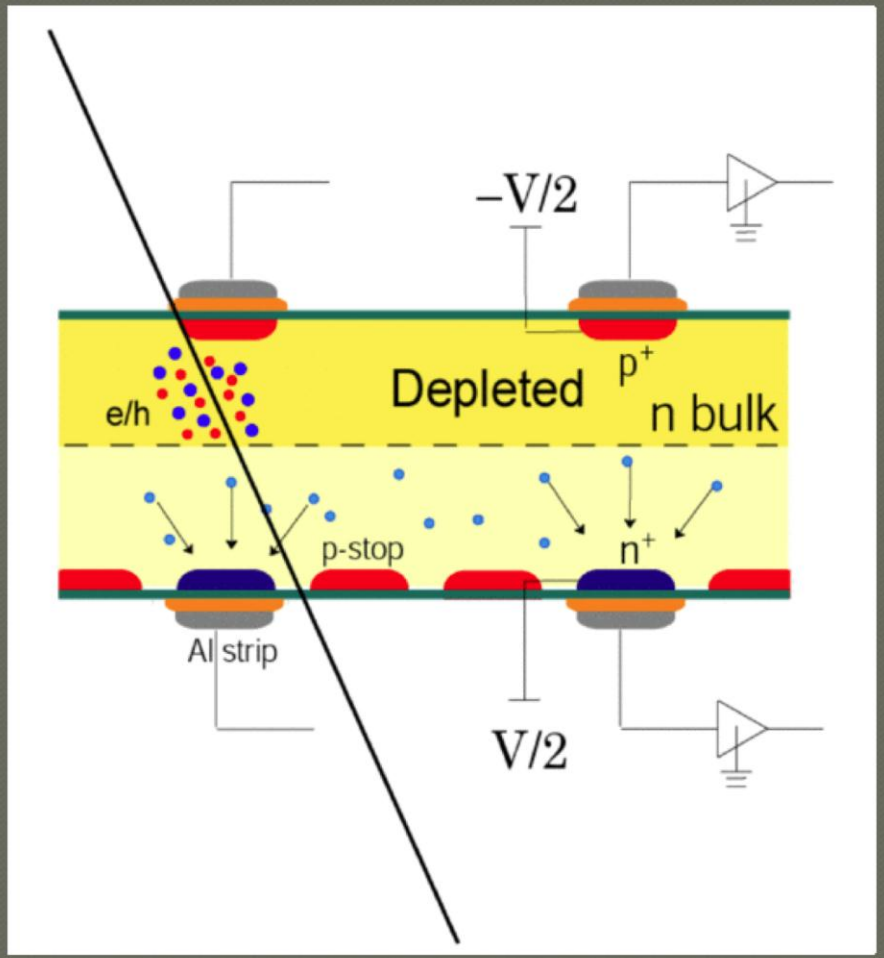


Assumptions: Complete donor removal (final V_{dep} independent of V_0);
$\tau_Y(20)$ = 3.2 & 6.5 yrs.

Aside – Double sided silicon strip detectors

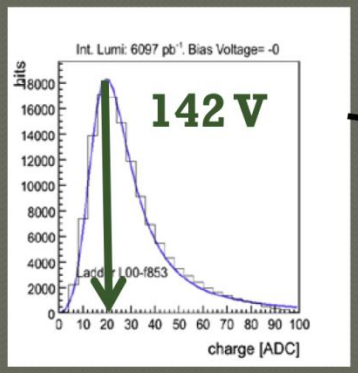
- First silicon strip detectors all used p strips, typically in n-bulk silicon. The backside contact was made with a single n+ implant, covered with metal.
- However, both sides can be segmented, and if the strips are not parallel to one another, the single plane can provide space points.
- n side strips must be isolated from one another
  - SiO_2 becomes positively charged & induces an n channel
- CDF SVX detectors are n-bulk with strips on both sides.

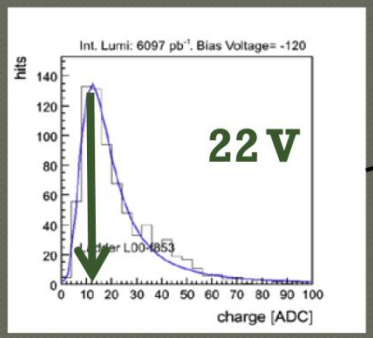
Depletion Voltage

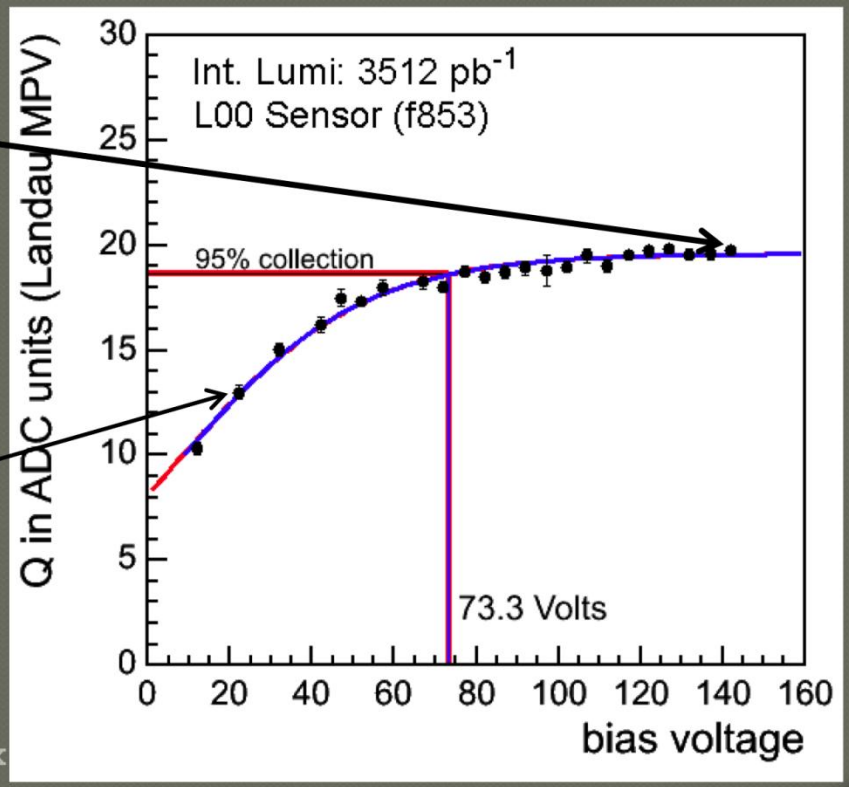


Depletion Voltage Measurement

- Plot peak charge for offline clusters as a function of bias voltage
- CDF defines depletion voltage as the minimum voltage that collects 95% of the charge at the plateau





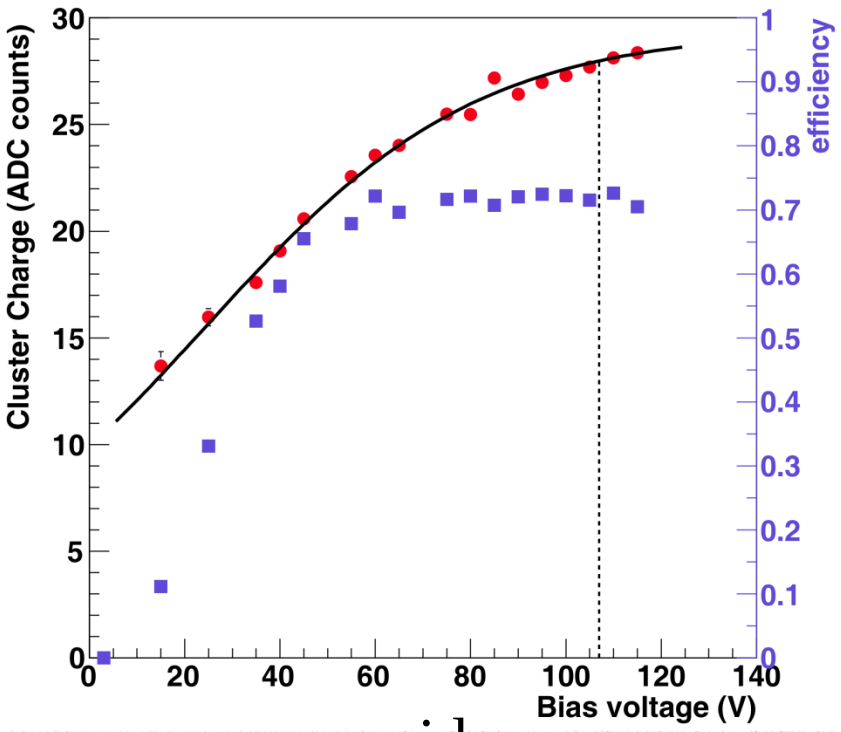


Implications of type inversion

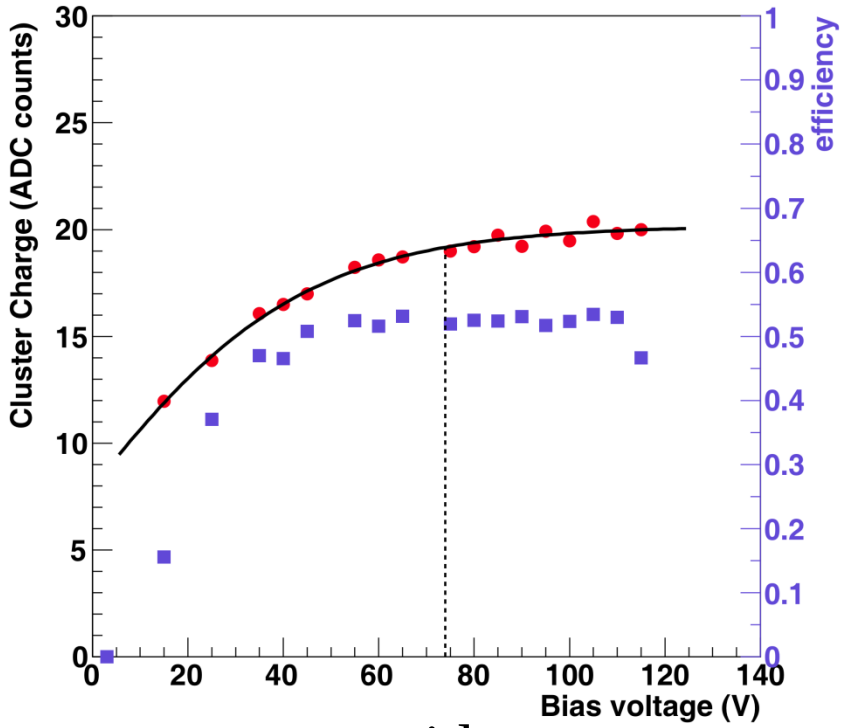
- When new, detectors deplete from the pn junction → n side strips see ~no signal until sensor is fully depleted
- The expectation was that after type inversion, depletion would occur first on the n side (at the new pn junctions) → p side strips would see ~no signal until sensor is fully depleted.

But… (shouldn't really have been a) surprise!

Even after heavy irradiation (well past type inversion), ***both*** p and n sides work at low voltage (under depleted) – the sensors act as though there are 2 diode junctions!



p side

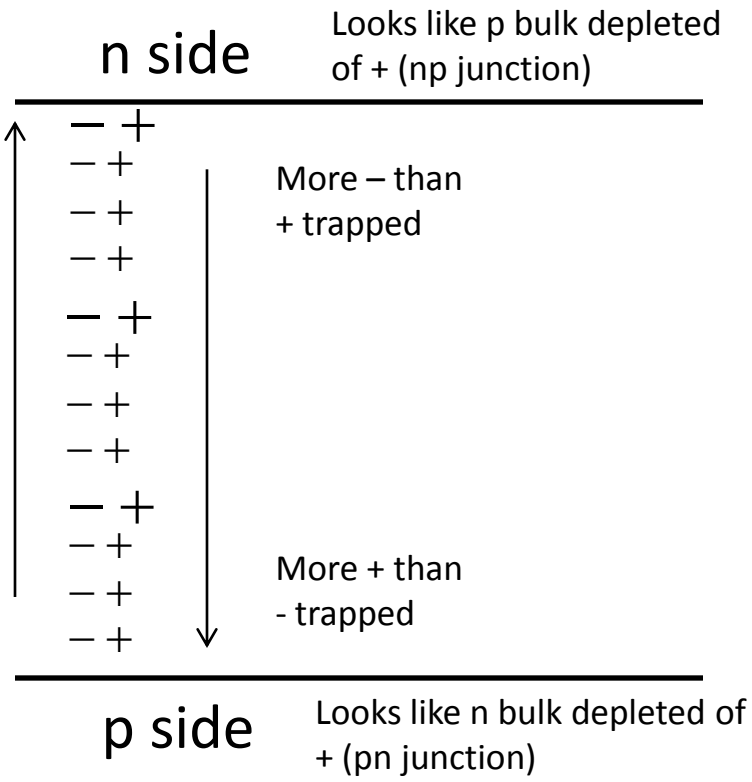


n side

(plots from Michelle Stancari)

What did we forget?

- When the number of defects (traps) is large, the space charge distribution (& therefor the E field) is determined ***primarily*** by trapping of leakage current carriers
- Two trap models
  - Eremin, Verbitskaya, Li (2002)
  - **Swartz, et al. (2006)**
    - Tuned to fit CMS pixel test beam results
    - Includes temperature dependence



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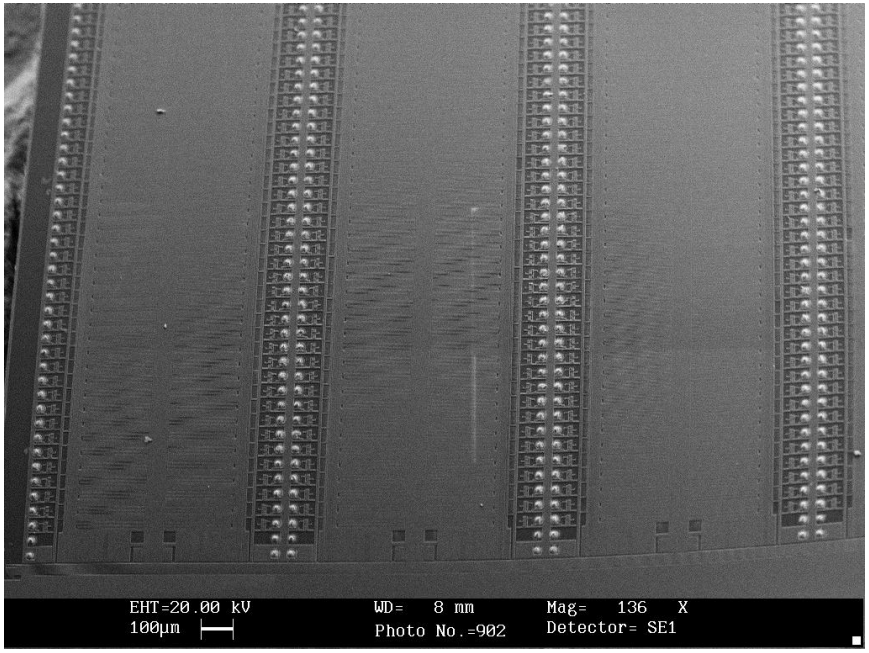
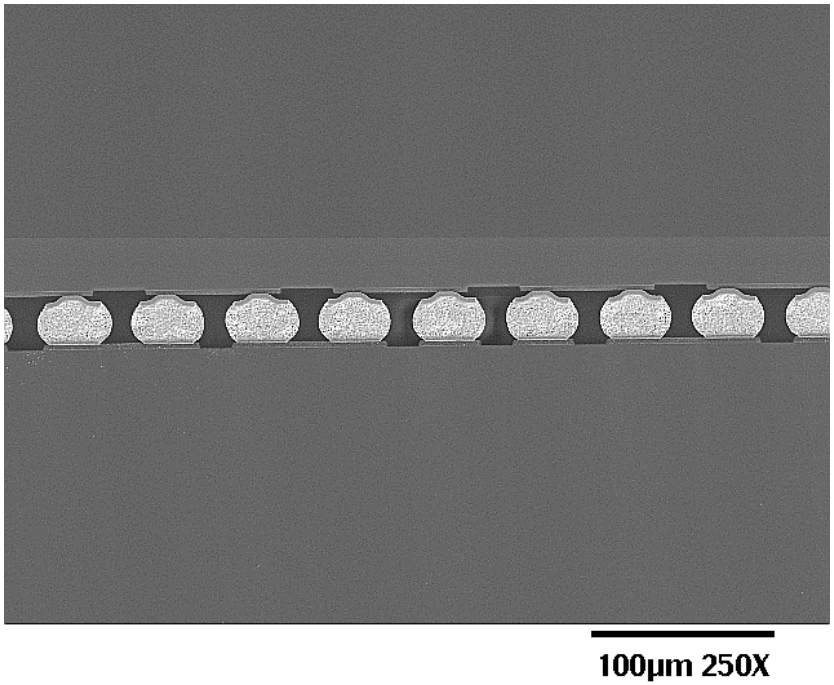
Types of Silicon Detectors

- Strip Detectors – used by everyone
- Hybrid Pixel Detectors – ATLAS, CMS, ALICE
- CCDs – ACCMOR, SLD, ILC??
  - (old standard for digital photography, astronomy)
- (Monolithic) Active Pixel Sensors
  - MAPS or APS – STAR, SuperB (Italy)?
  - (new standard for digital photography)
- 3D
  - Sensors – ATLAS, CMS?
  - ICs – CMS?, ILC??

Hybrid Pixel Detectors

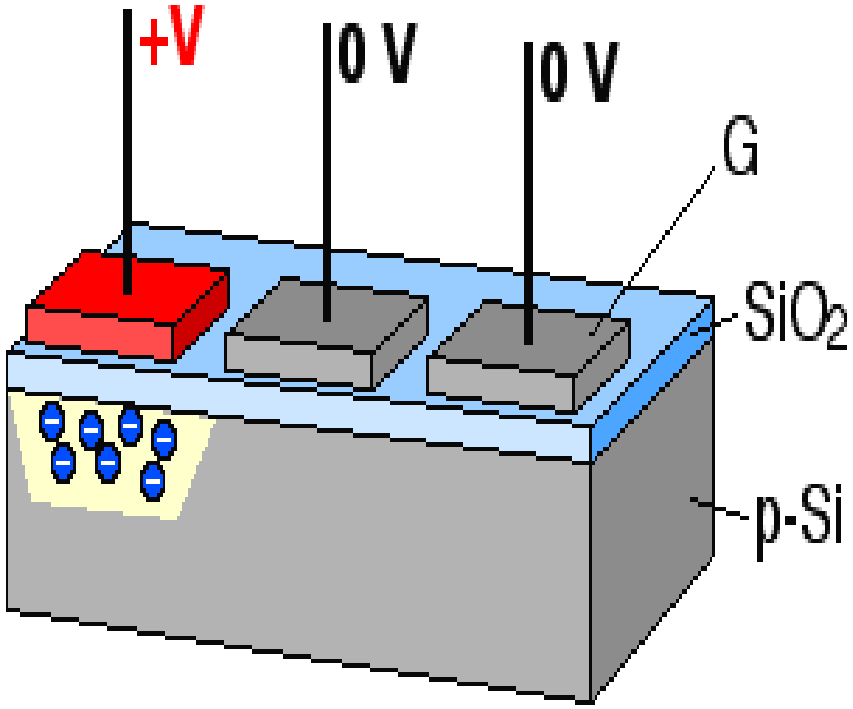
- Sensor & readout IC separately optimized (sensor is like single sided SSD with very short strips)
- Enabling technology for hybrid pixel detectors = bump bonding
- Now installed in ATLAS, CMS, & ALICE





CCDs

- Charge usually collected by diffusion in a thick epitaxial (very pure) silicon layer
- Charge held under a biased electrode in a shallow depleted region
- Charge shifted from pixel to pixel and read out through a buffer amplifier (1 per device, 1 per quadrant, 1 per column…)
- Much more from Juan Estrada later in this school.

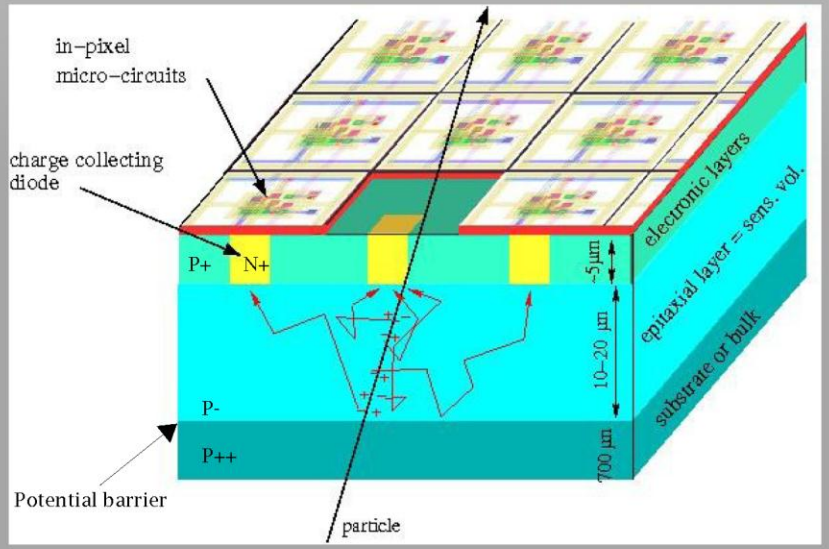


From Wikimedia Commons

MAPS, the basics

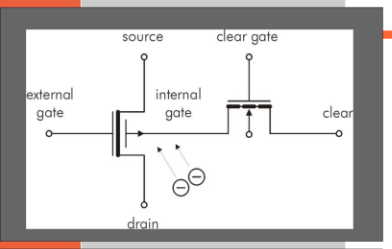
(Jerome Baudot – Vertex 2010)

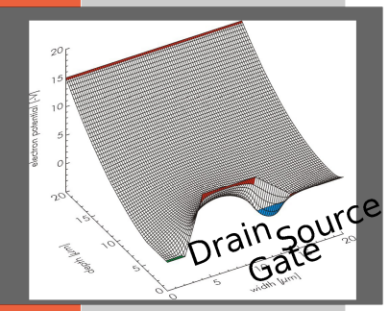
- Technology
  - ✗ Industry standard for ICs
  - ✗ All processes not optimized
    - ➔ Epitaxial layer thickness
    - ➔ # metal layers
    - ➔ Nwell – Psubstrate junction



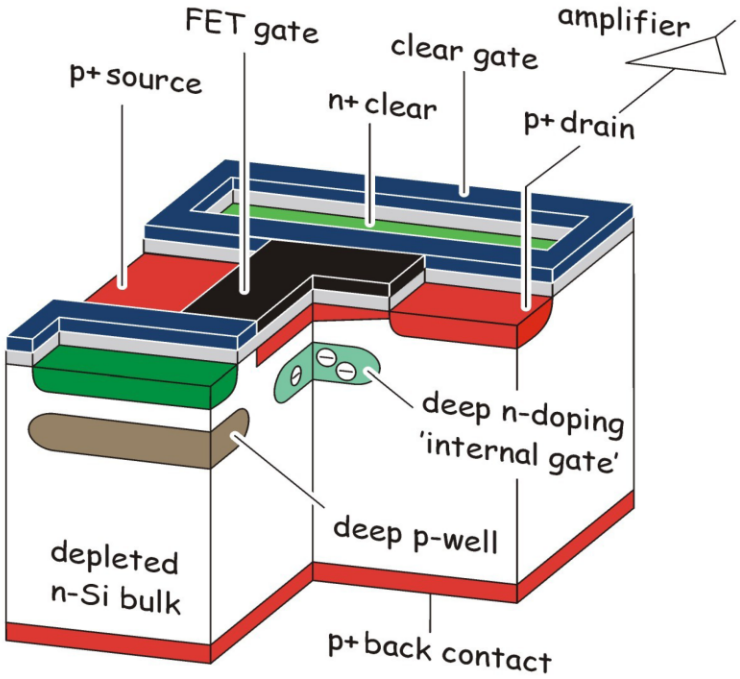
- Intrinsically thin sensors
  - ✗ sensitive layer ~10-20 µm
    - ➔ Small MIP signal, few 100 e- per pixel → requires low pixel noise *O*(10 e-)
  - ✗ Substrate almost useless
    - ➔ Few µm enough, total thickness could reach 20 µm
  - ✗ Monolithic & active
    - ➔ No external IC required in vicinity

The DEPleted Field Effect Transistor





- **Amplification stage integrated in the sensor**
  - Very low noise
- **Fully depleted, high resistivity silicon sensor**
  - Fast and complete charge collection



in-pixel amplification

characterized by g_q (pA/e^-)

noise performance!

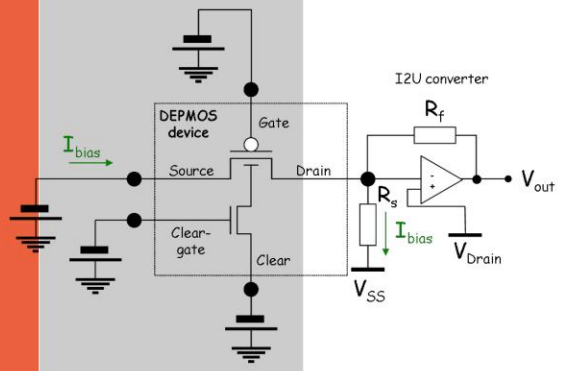
thin sensors!

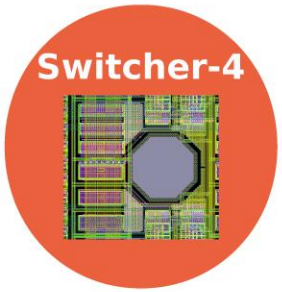
Signal collected when pixel is "off"

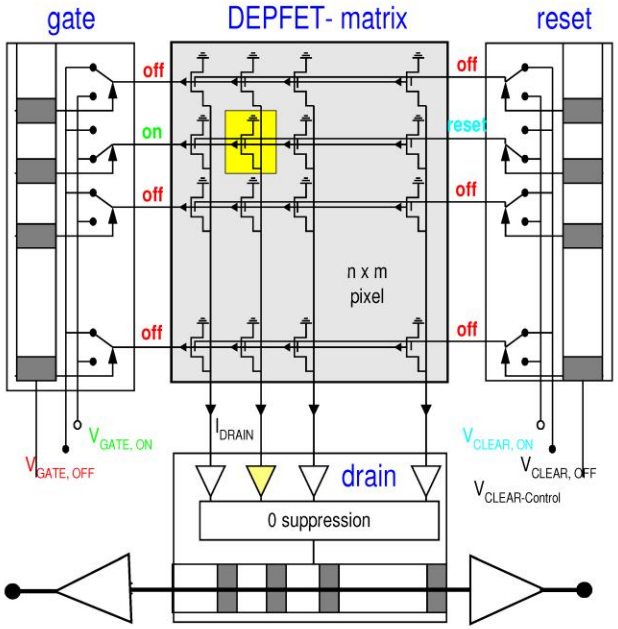
power consumption!

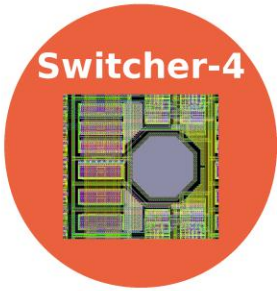
Clear the signal

A DEPFET active pixel detector





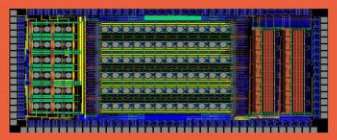




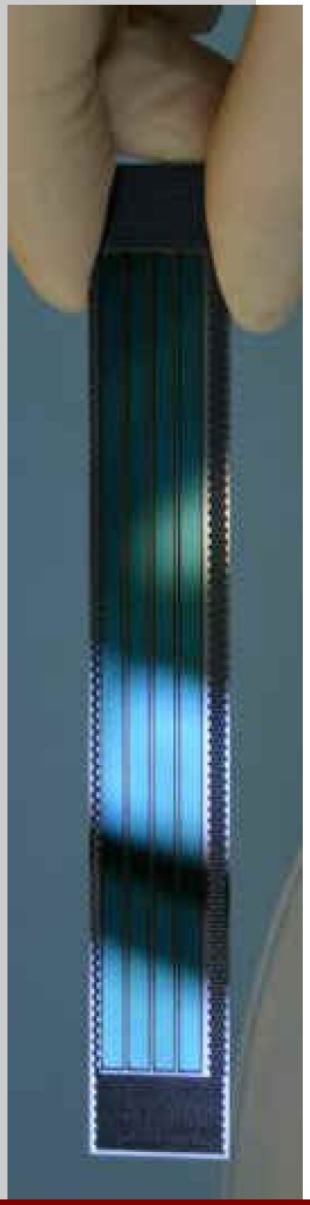
Row wise read-out ("rolling shutter")

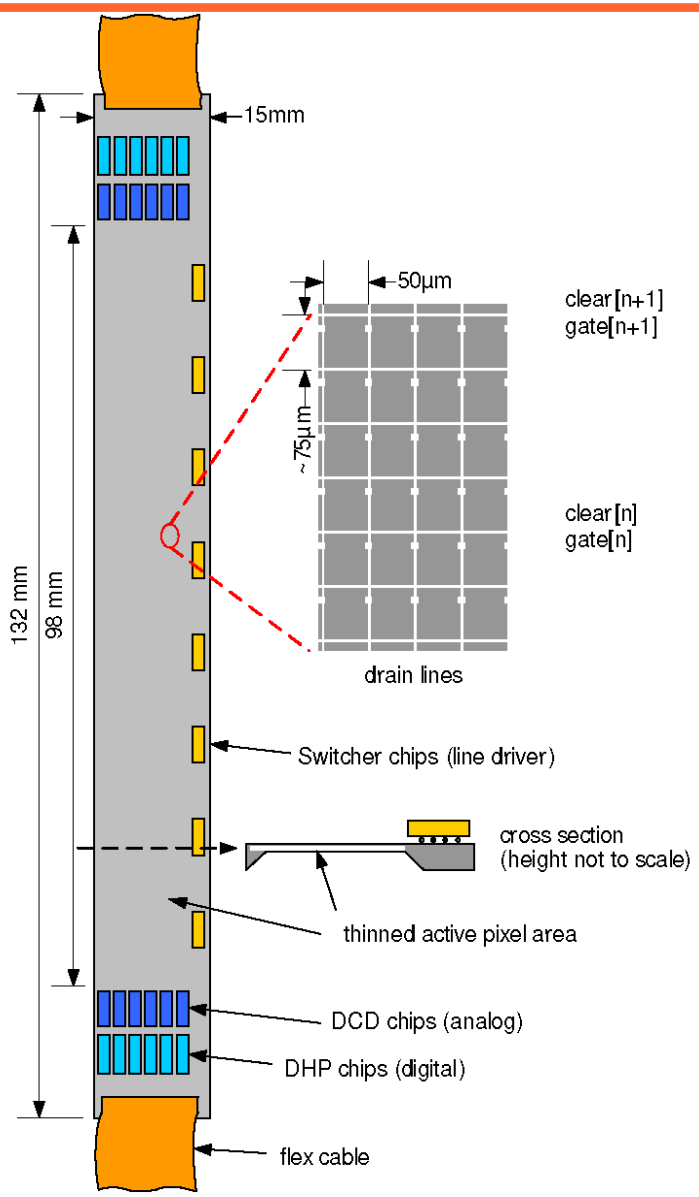
- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal
- Low power consumption
- two different auxiliary ASICs needed
- limited frame rate
- cap. load at the f/e adds noise

DCD
Drain Current Digitizer



The all-silicon module





The all-silicon module

- The DEPFET sensor is self-supporting
- It can be thinned
- Auxiliary electronics located on end- of sensor (readout) and balcony (steering)
- One material – uniform (and small) thermal expansion

✔ Small pixels, excellent spatial resolution
✔ Good signal/noise from thin device
✔ Low power consumption

Vertex detector for future colliders

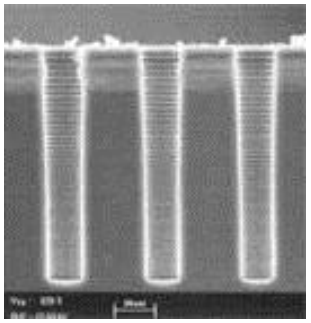
3D Sensors and ICs

- The next high impact enabling technology may be come from the same IC technologies that are enabling a revolution in micromachining (MEMS)

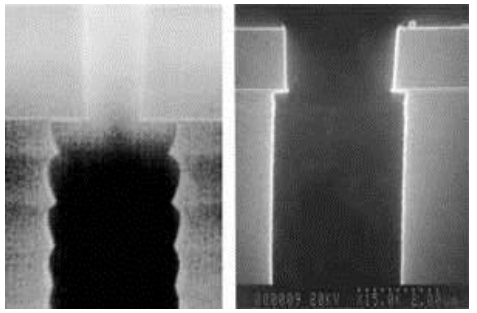
TSV Hole Fabrication Techniques

TSV = Through Silicon Via

- Etching
  - Deep Reactive Ion Etch (DRIE) is used to etch holes in silicon.
    - The most widely used method for forming holes in silicon
    - The process tends to form scalloped holes but can be tuned to give smooth walls.
    - Small diameter holes (1 um) and very high aspect ratio (100:1) holes are possible.
  - Plasma oxide etch is used to form small diameter holes in SOI processes. This process used by MIT LL. [2]
    - Since the hole is in an insulating material, it does not require passivation before filling with conducting material.
  - Wet etching
    - KOH silicon etch give 54.7^0 wall angle
- Laser Drilling –
  - Used to form larger holes (> 10 um)
  - Can be used to drill thru bond pads and underlining silicon with 7:1 AR
  - Toshiba and Samsung have used laser holes for CMOS imagers and stacked memory devices starting in 2006.



SEM of 3 Bosch process vias [1]

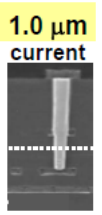


SEM close up of walls with/without scallops in Bosch process [1]

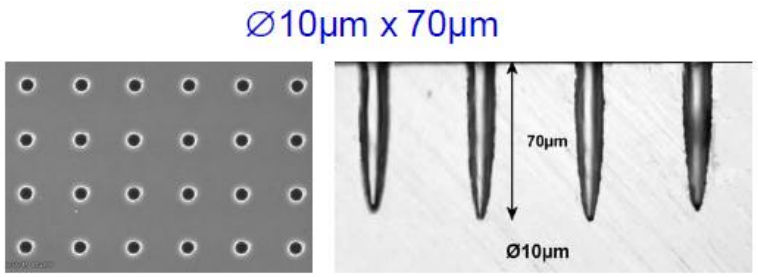
Plasma Oxide etch

1024×1024, 8-µm pixel visible image sensor

64 x 64, 50-µm pixel LADAR



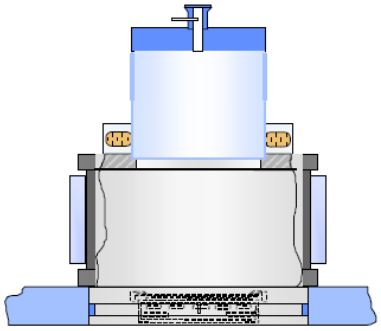
3D via test chain

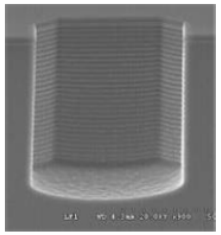


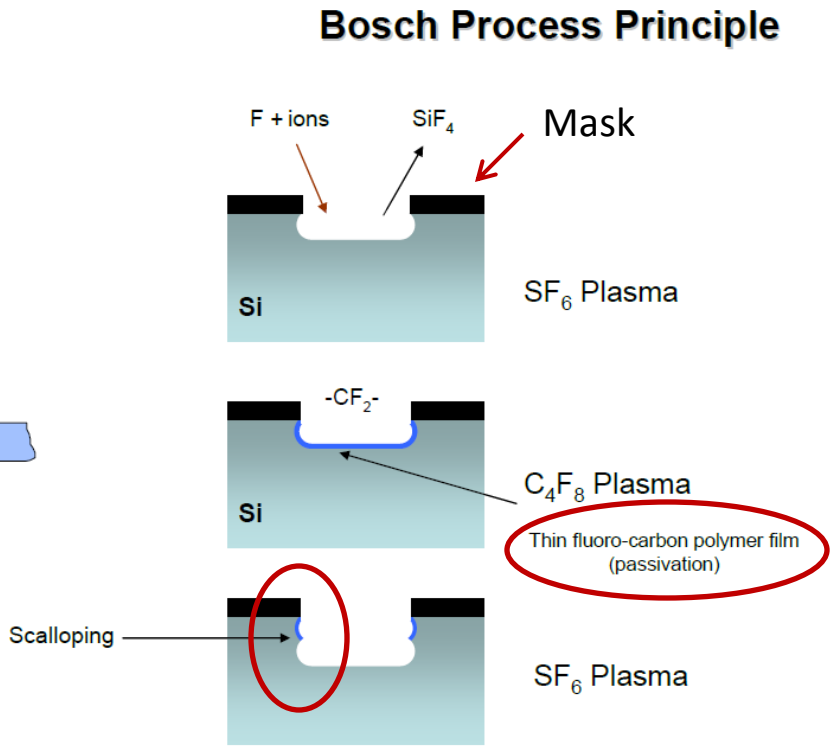
Laser drilled holes by XSIL [3]

DRIE for Through Silicon Vias [4]

- Holes are formed by rapidly alternating etches with SF_6 and passivation with C_4F_8
- Any size hole is possible (0.1 -800 um)
- Etch rate is sensitive to hole depth and AR (aspect ratio).



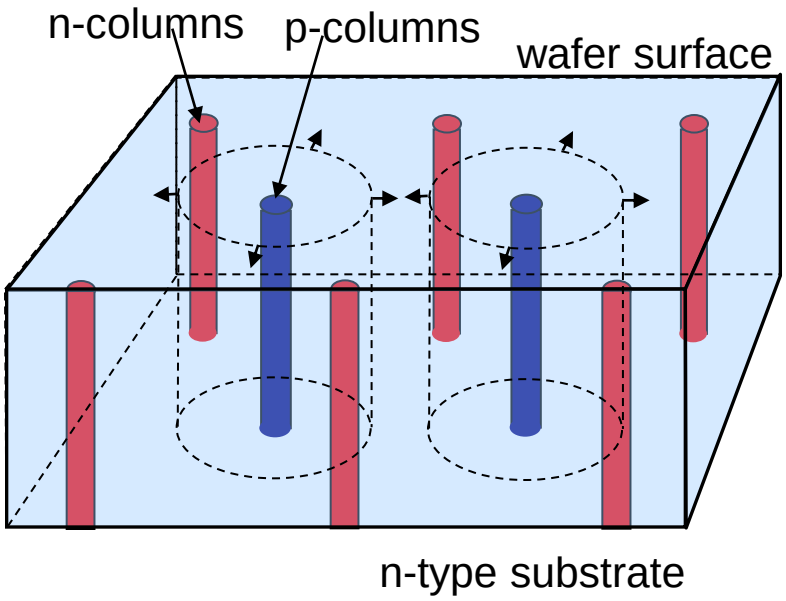




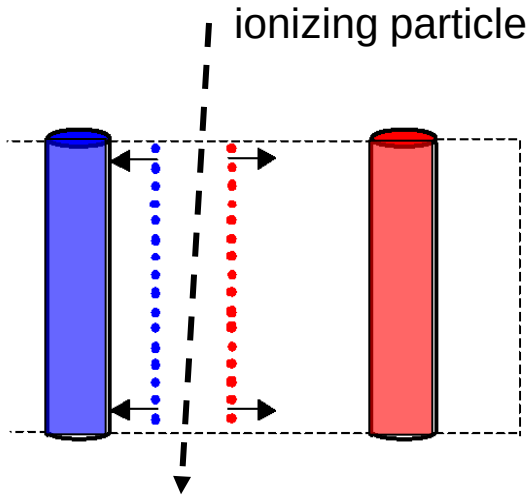
Ray Yarema Vertex 2010

(G.-F. Dalla Betta – Vertex 2007)

"Standard" 3D detectors - concept



[Parker et al., NIMA395 (1997)]



Lateral depletion and carrier drift, charge collection in a very short time

Distance between *n* and p electrodes can be made very short

➡ **extremely radiation hard detector**

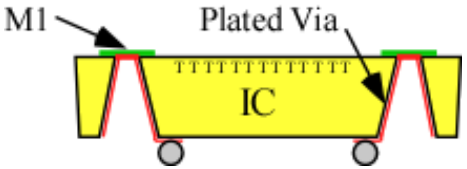
(low full depletion voltage and high CCE even at very high fluences)

Drawbacks:

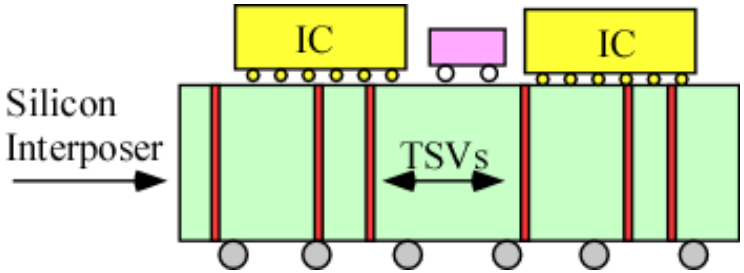
- electrodes are (partially) dead regions
- feasibility of large scale production still to be assessed

3D Integration Platforms with TSVs

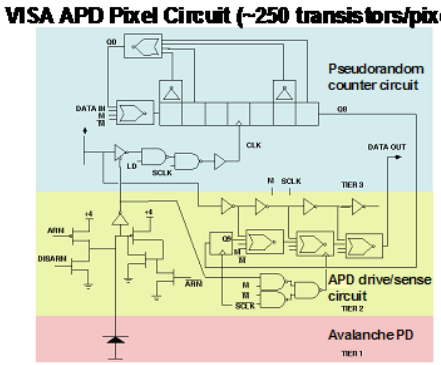
- 3D wafer level packaging
  - Relatively large vias on a coarse pitch added at wafer level
  - Usually for peripheral connections
  - Backside contact allows stacking of chips or adding a sensor on top
  - Low cost
  - Small package
- 3D Silicon Interposers (2.5D)
  - Built on blank silicon wafers
  - Provides pitch bridge between IC and substrate
  - Can integrate passives
- 3D Integrated circuits
  - Small vias added at wafer level permit internal chip connections between tiers
  - Opens door to multilevel high density vertical integration
  - Reduces interconnect paths between circuit elements

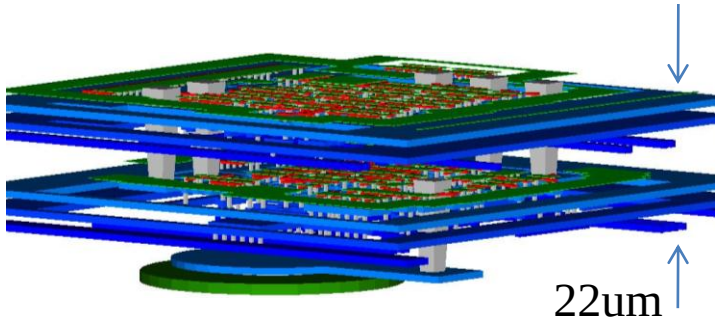


3D Wafer level package



3D Silicon interposer





MIT LL 3D integrated APD Pixel Circuit [8]

Ray Yarema TIPP 2011, Chicago

3D ICs in HEP

- 3D Consortium (http://3dic.fnal.gov)
  - CPPM, IPHC, LAL, LPNHE, IRFU, CMP, Bergamo, Pavia, Perugia, Sherbrooke, INFN (Bologna, Pisa, Rome) Bonn, AGH, Fermilab
- Multi-Project Wafer service now offered by MOSIS, CMP, and CMC (US, Europe, Canada)

Challenges of the Future

- High Luminosity LHC
  - Radiation tolerance (~10^{16}/cm^2 for pixels, 10^{15}/cm^2 for strips; ~20x current)
  - High hit rate (up to 1.5 GHz/cm^2 in pixels)
  - High track density (200 or more spectator events)
- e+e- colliders
  - Extremely low material (minimize multiple scattering)
    - Requires very low average power
  - Extremely good position resolution (ILC goal is ~3 microns)

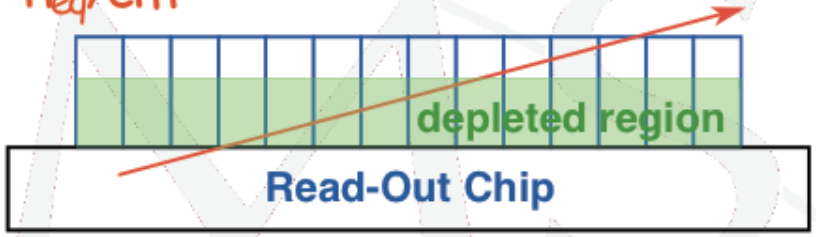
Backup slides

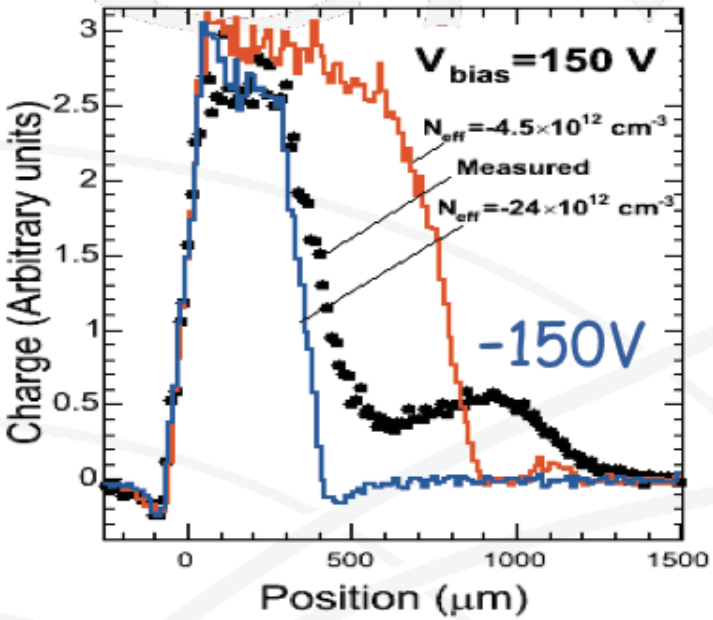
Charge sharing (optimizing position resolution)

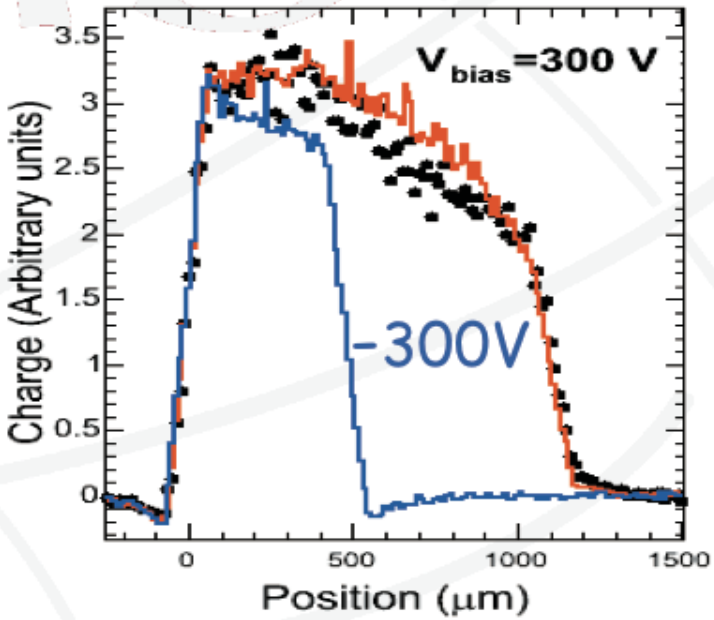
- DC coupled (pixels):
  - Charge in pixel ~ track length in pixel
  - If every track crosses 2 pixels, then position = center of gravity of 2 charge measurements (pulse heights)
  - If many tracks cross only one pixel, then position is always near the boundary when 2 are on → need “eta function” (or lookup table)
- AC coupled (strips):
  - Charge sharing is combination of track length in strip and capacitive coupling with neighboring strips → center of gravity approximation is often all that’s needed.

Irradiated Data vs Simulation

Comparing grazing-angle charge collection profiles of real and simulated data at $\Phi_1=5.9\times10^{14}\ n_{eq}/cm^2$







T=-10C

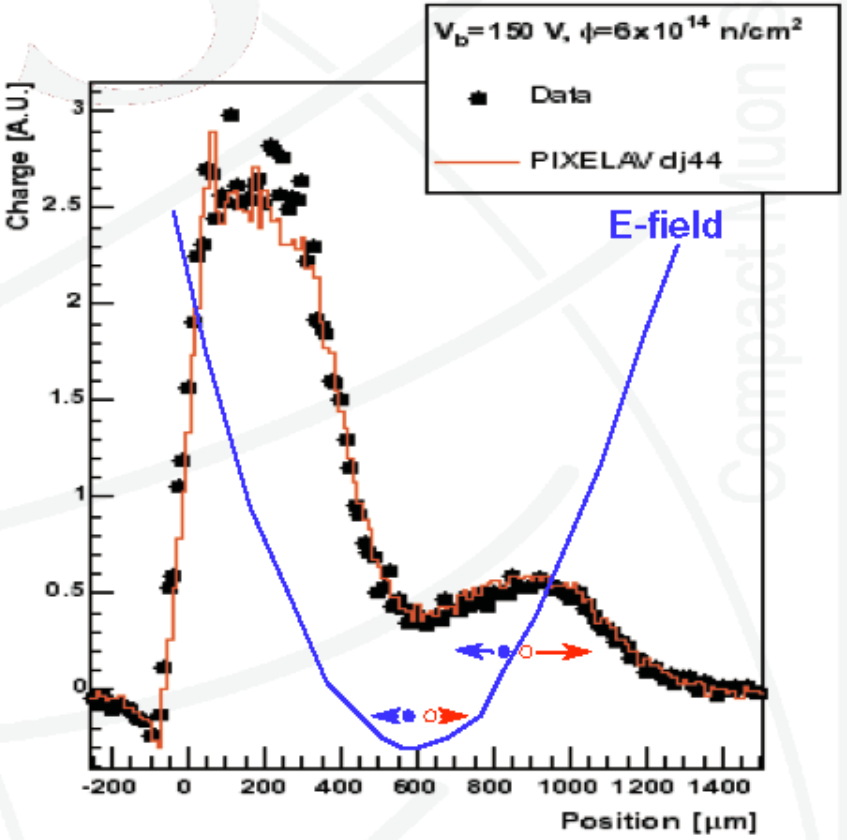
- -300V data are well described by $N_{eff}=4.5\times10^{12}cm^{-3}$ p-
- width of -150V peak requires $N_{eff}=24\times10^{12}cm^{-3}$ p-
  - tail not described
- Constant N_{eff} and linear E-fields are ruled out!

(Morris Swartz – SNIC06)

The "Wiggle"

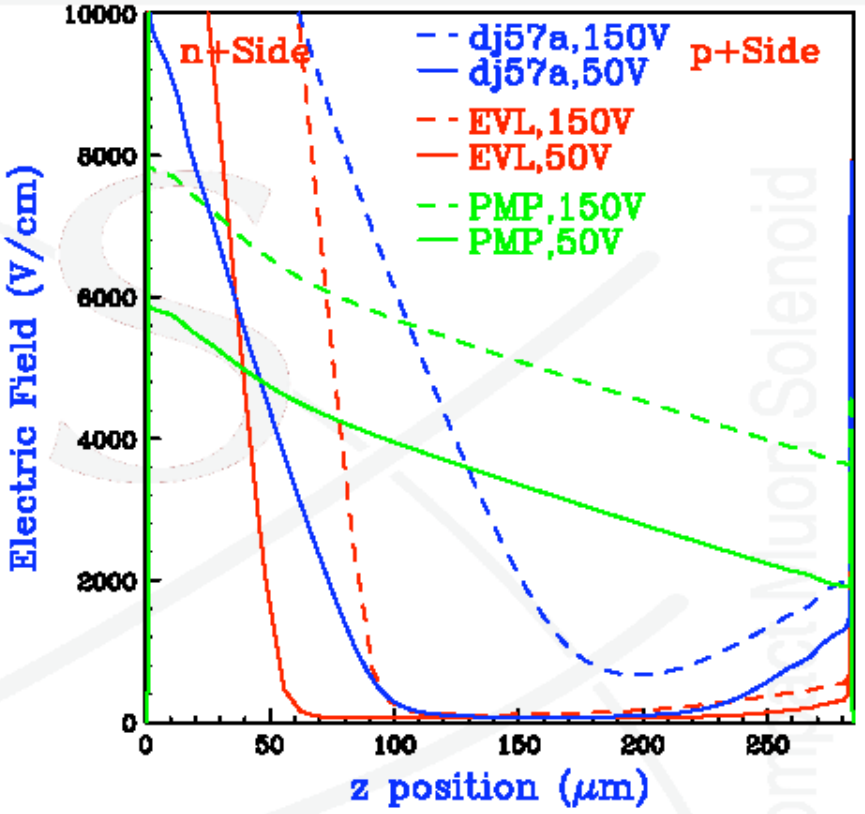
The charge collection profiles show a "wiggle" at low bias:

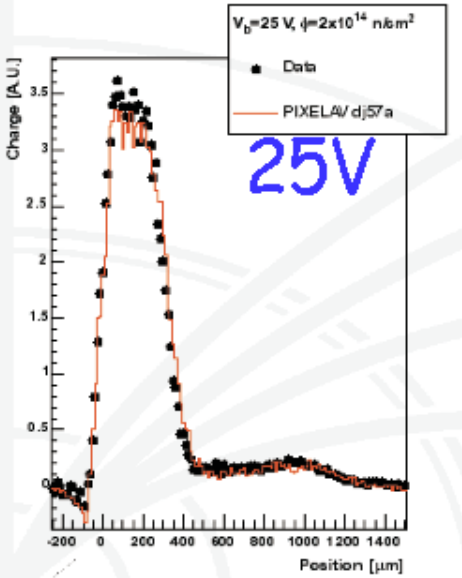
- signature of a doubly-peaked electric field:
  - e-h pairs deposited near field minimum separate only a little before trapping, produces local minimum
  - the apparently "unphysical" bump is caused by collection of holes in the higher field region near the p+ implant (e's drift into low field region and trap)

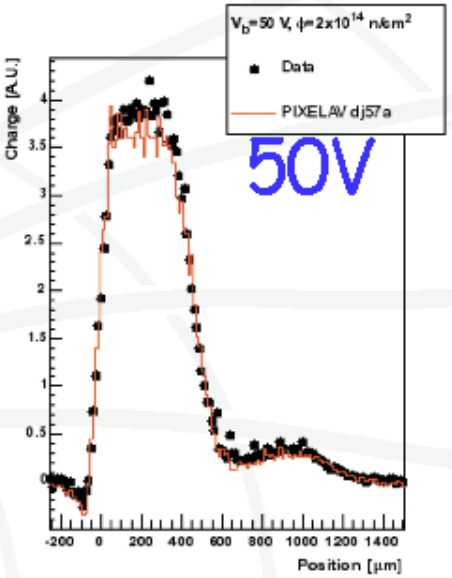


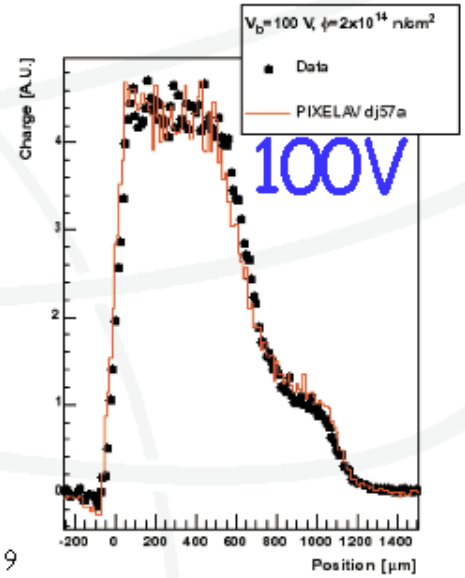
Best fit to 2.0×10^{14} n_{eq}/cm^2 is labelled dj57a

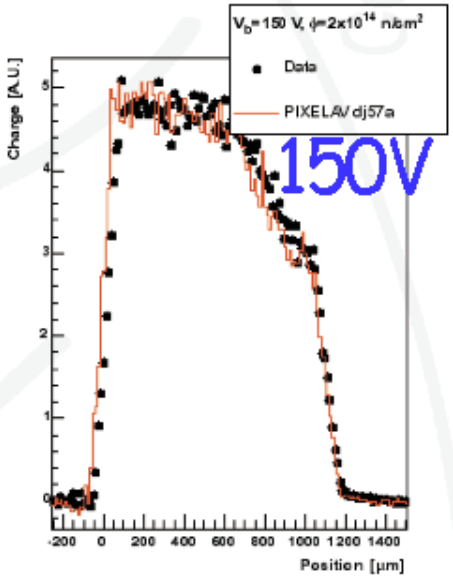
- $N_A/N_D=0.68$
- $\sigma_{Ah}/\sigma_{Ae}=0.25$, $\sigma_{Dh}/\sigma_{De}=1.00$,
- E-field still doubly-peaked (more than EVL prediction)
- Also compare with PMP model





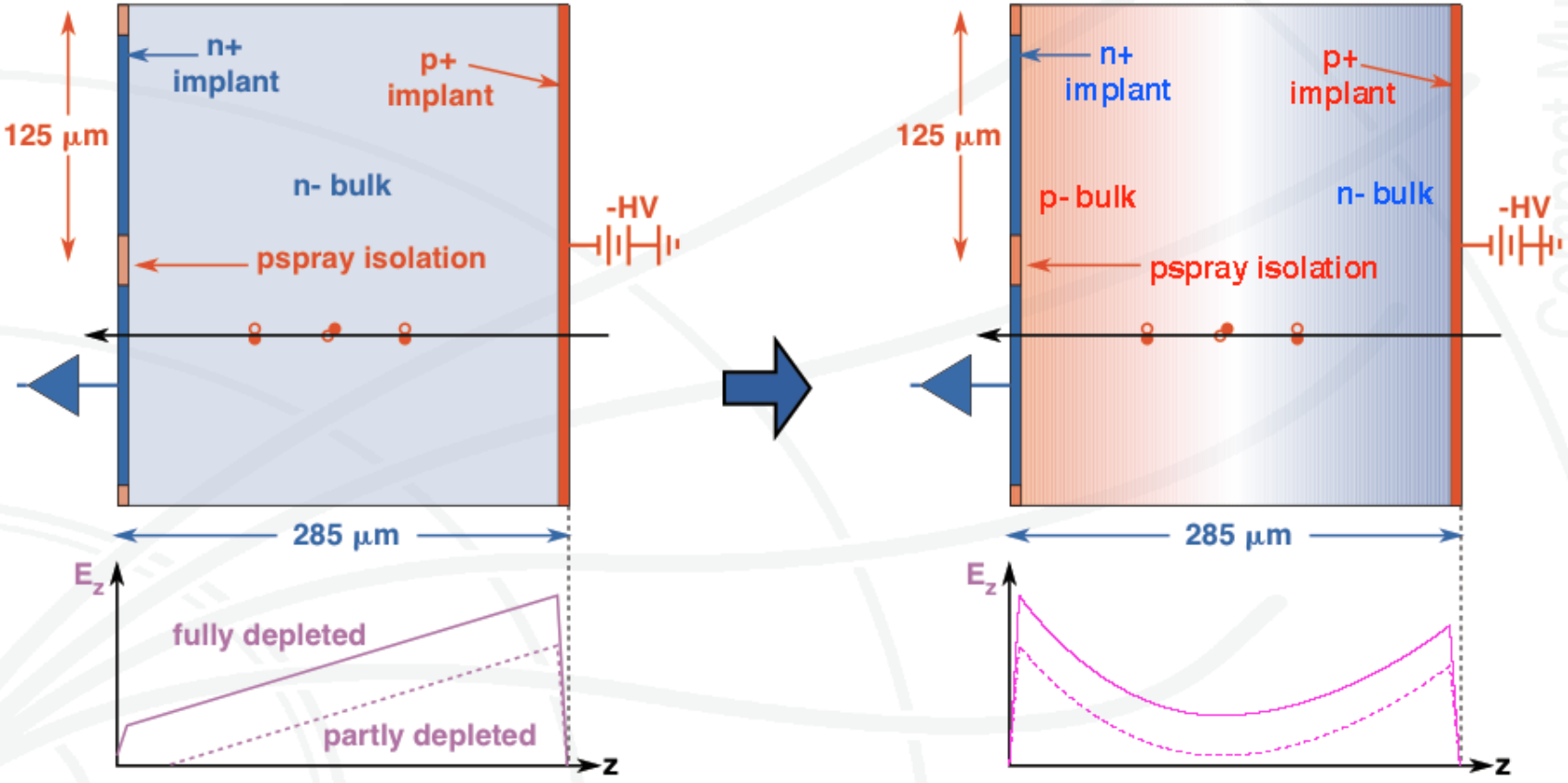






Conclusions

- It is clear that a two-peak electric field is necessary to describe our charge collection data even at low fluence
  - Usual model of type inversion after irradiation is wrong:
    - only ~1/2 of the junction inverts, ρ_{eff} is not constant

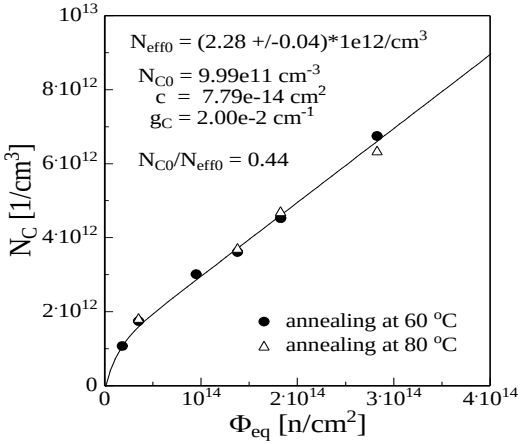


Parameterization of radiation damage to oxygenated Si:

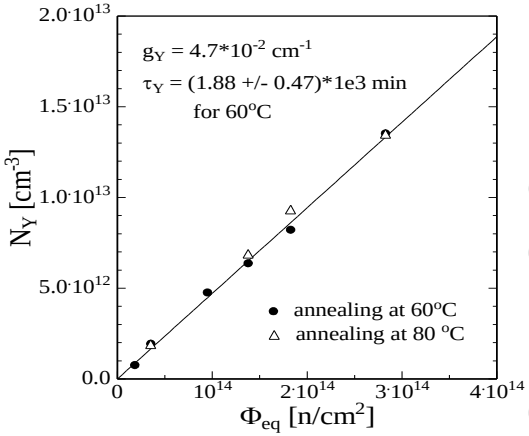
Donor removal

Acceptor generation

Neutrons, constant term,oxy Si



n, reverse annealing term, oxy Si



$$N_C(n) = N_{C0}(1-\exp(-c\Phi_{eq})) + g_C\Phi_{eq}$$

N_{C0} = (initial dopant concentration)x0.44

c = 7.79E-14cm^2 ≈ 1/1.3E13cm^{-2}

g_C = 2.00E-2cm^{-1}

$$N_Y(n)=g_Y\Phi_{eq}$$

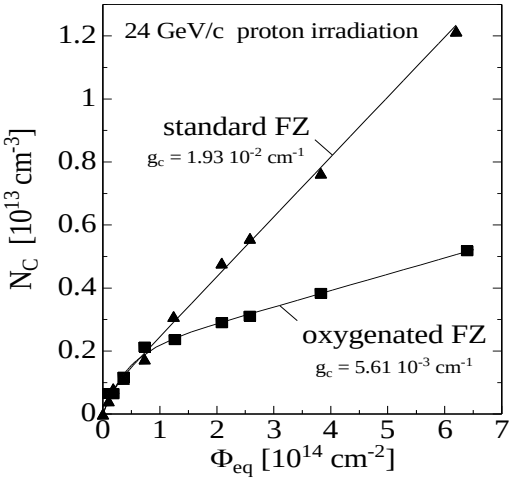
g_Y = 4.7E-2cm^{-1}

Note:

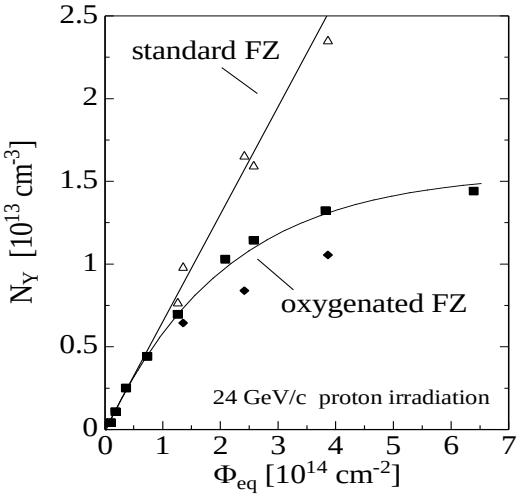
1) There are large variations in reported donor removal parameters (N_{C0}/N_0 & c).

2) Donor removal occurs rather quickly.

Protons, constant term



p, reverse annealing term



$$N_C(p)=N_{C0}(1-\exp(-c\Phi_{eq})) + g_C\Phi_{eq}$$

N_{C0} = (initial dopant concentration)x1

g_C = 5.61E-3cm^{-1}

$$N_Y(p)=1.55E13(1-\exp(-\Phi_{eq}/2.2E14)$$

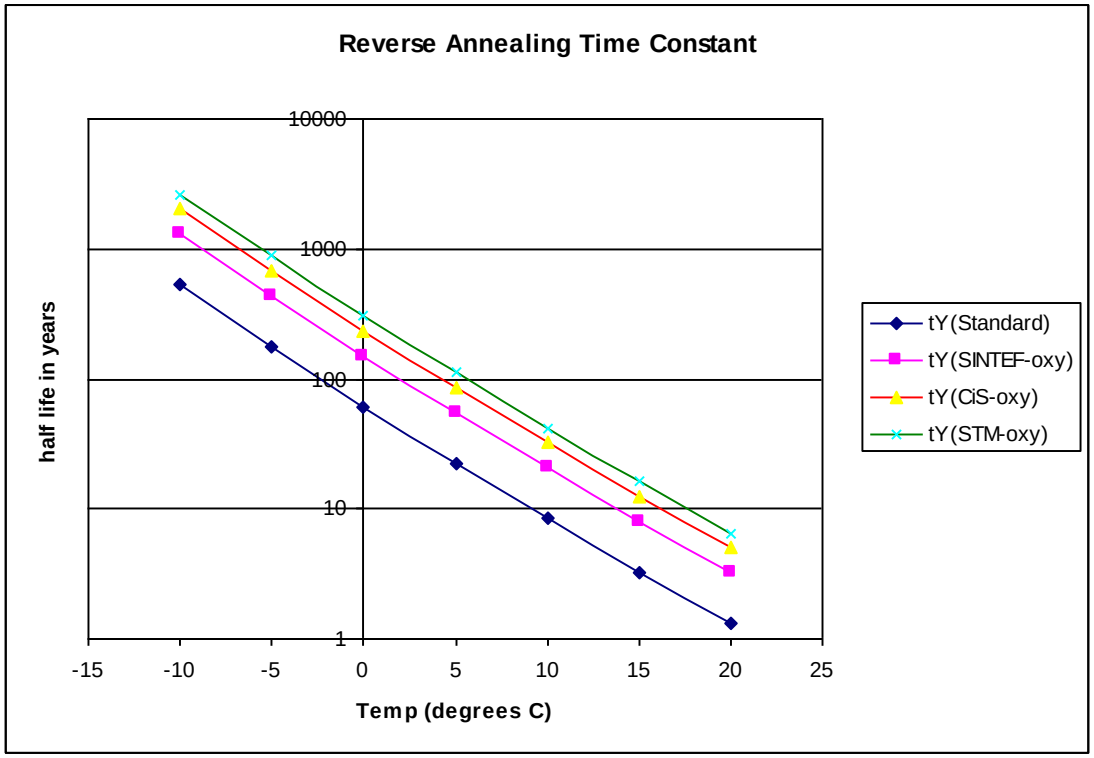
Plots are from the 3rd ROSE status report.

Reverse Annealing

Time dependence = $(1 - (1/(1+t/\tau_Y)))$

Temperature dependence:

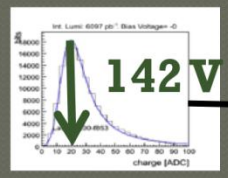
$\tau_Y(T) = \tau_{Y20}\exp((1.33/8.617E\text{-}5)(1/293.15 - 1/T))$

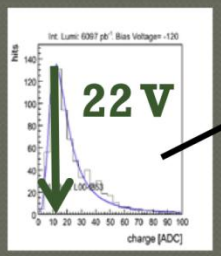


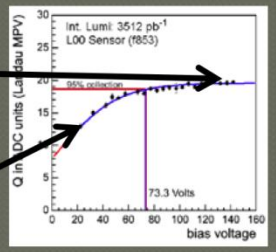
Depletion Voltage Measurement

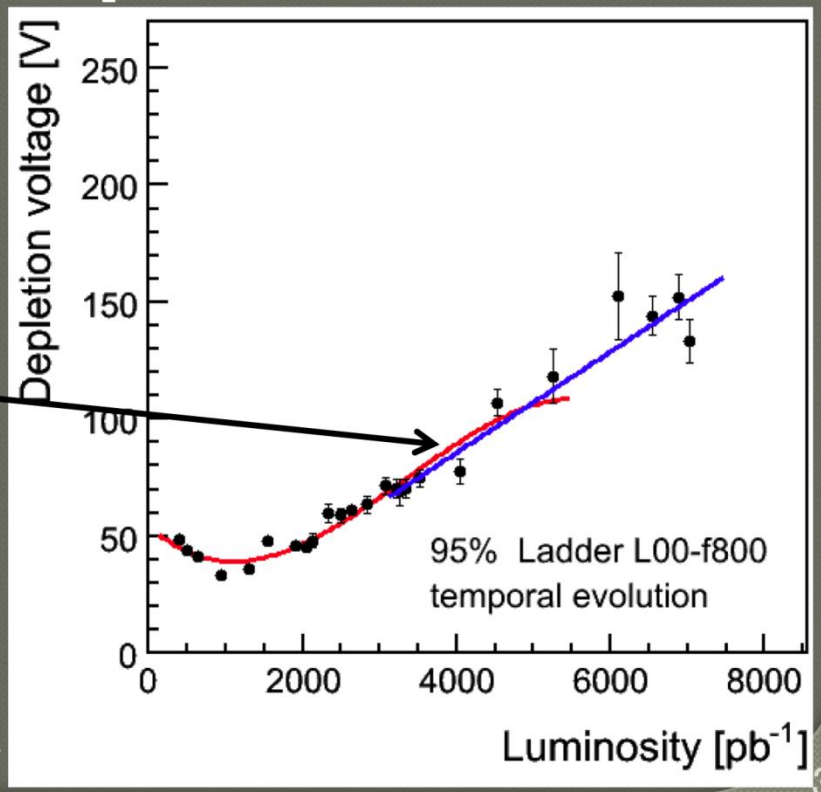
- Plot collected charge for different bias voltages
- Determine depletion voltage as the minimum voltage that collects 95% of the charge at the plateau
- Extrapolate into the future

  3rd order polynomial fit around the inversion point, linear fit after









(aside) Getting a Signal From Mobile Charges in a Semiconductor Detector

- Many mobile charge carriers are produced by energy deposition in the crystal.
- There must be a region in which an E field exists so that motion of the mobile charge will induce a signal that can be amplified (or charge collected/stored).
- Usually, this is accomplished by creating a volume that is depleted of mobile charge (depletion region) and can therefor support an E field.
  - With a diode junction
  - With an electrode capacitively coupled to the silicon
- Charge can also be collected from region of zero field (if it diffuses to the region of non-zero field)
  - Most CCDs and MAPS have very small depletion regions and collect electrons by diffusion in a thin epitaxial layer (electrons are trapped in the layer by a field at the p/p+ boundary with the substrate)
- E field can also depend on dc current
  - Radiation damaged silicon traps mobile charges produced thermally in the bulk; trapped leakage current produces space charge regions that are large near both sides of the sensor ("double junction" described by a number of authors)
  - Novel MAPS proposed by De Geronimo, et al. (NIM A 568 (2006) 167): applied voltage drives large dc current (composed of holes only) between p implants. Resulting E field helps collect mobile electrons created by particle being detected.

Further use of IC Technology Required by Collider Experiments

- Key enabling technology = ASIC (custom chip)
  - fan out to bulky FE electronics no longer required
- First custom readout chip: MarkII Microplex (1984)
  - LBL design, Stanford fab: 5μ NMOS (single metal, single poly)
- LEP experiments
  - MPI-Munich CAMEX64 (ALEPH), Fraunhofer (Duisburg) fab: 3.5μ CMOS
  - Rutherford Lab (OPAL & DELPHI), Plessy fab: 5μ, then 3μ CMOS
    - Correlated double sampling (reduced noise)
- CDF
  - LBL designed SVX
    - First IC designed for high rate (pedestal subtraction & zero suppressed read out)
    - First HEP ASIC prototyped & produced through MOSIS
- MANY MORE

Depletion Voltage in terms of bulk resistivity

- Bulk resistivity is related to the concentration of n-dopants, the electron mobility, the concentration of p-dopants, and the hole mobility.
- For n-bulk containing only n-dopants

$$\rho = {}^{1}/_{Nq\mu_e}$$

ρ = resistivity in Ωcm

N = Number of n-dopants per cm^3

μ_e= 1300 cm^2/V-sec & q=1.6E-19C

➔ N = $10^{12}/cm^3$ corresponds to ρ = 4630 Ωcm